TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS

TEES

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CHAPTER 1-SECTION 1
ELECTRICAL TERMONOLOGY

1.1.1 Glossary of Terms

A	Amperes
AASHTO	American Association of State Highway and Transportation Officials
AC	Alternating Current
AC+	120 Volts AC, 60 hertz ungrounded power source
AC-	120 Volts AC, 60 hertz grounded return to the power source
AGENCY	Purchasing Government Agency
ANSI	American National Standard Institute
API	Application Program Interface
ASCII	American Standard Code for Information Interchange
Assembly	A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules
ASTM	American Society for Testing and Materials
ATC	Advanced Transportation Controller
AWG	American Wire Gage
bps	bits per second
Big Endian	The sequencing of byte order in memory such that the most significant byte is stored at the lowest memory address, with the next byte in significance stored at the next memory location, and so on.
C	Celsius
C Language	The ANSI C Programming Language
Cabinet	An outdoor enclosure generally housing the controller unit and associated equipment
Certificate of Compliance	A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications
Channel	An information path from a discrete input to a discrete output
CIA	CMS Controller Isolation Assembly
CIP	CMS Interface Panel
CMOS	Complementary Metal Oxide Semiconductor
CMS	Changeable Message Sign
CMS SYSTEM	Includes Controller Unit, Model 334C Cabinet, Interconnect Harnesses, CMS and other associated equipment required to operate the system.
Component	Any electrical or electronic device

Contractor	The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the AGENCY, as party(s) of the second part or legal representative
Controller Unit	That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly
CPDA	CMS Pixel Driver Assembly
CPDM	CMS Pixel Driver Module
CPMM	CMS Pixel Matrix Module
CPU	Central Processing Unit
CR	ACIA Control Register
CRC	Cyclic Redundancy Check
CTS	Clear To Send
DAT Program	The AGENCYs Diagnostic and Acceptance Test Program
Daughter Board	(from TechEncyclopedia) A Printed Circuit Board that plugs into another Printed Circuit Board to augment its capabilities
DB	Decibel
DBa	Decibels above reference noise, adjusted
DC	Direct Current
DCE	Data Communications Equipment
DIN	Deutsche Industrie Norm
DMA	Direct Memory Access
DTA	Down Time Accumulator
DTE	Data Terminal Equipment
DPST	Double Pole Single Throw
EG	Equipment Ground
EIA	Electronic Industries Association
EMI	Electro Magnetic Interference
Engineer	The AGENCY director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them
EPROM	Ultraviolet Erasable, Programmable, Read Only Memory Device
EEPROM	Electrically Erasable, Programmable, Read Only Memory Device
Equal	Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device
ETL	Electrical Testing Laboratories, Inc.
FCU	Field I/O Controller Unit.
Firmware	A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM

FLASH	An IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features
FPA	Front Panel Assembly
HDLC	High-Level Data Link Control
HEX	Hexadecimal
Hz	Hertz
IC	Integrated Circuit
I.D.	Identification
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
IPI	Initial Protocol Identifier
ISP	Information Service Provider, this is funny it never was a service provider!!!!!
ISO	Short for "Isolated" and signifies that two or more power supplies each have different reference grounds.
ISO/IEC	International Standards Organization
ITE	Institute of Transportation Engineers
ITS	Intelligent Transportation Systems
Jumper	A means of connecting/disconnecting two or more conductive points by soldering/desoldering a conductive wire.
KB	Kilobytes
Laboratory	The established laboratory of the AGENCY or other laboratories authorized by the AGENCY to test materials involved in the contract
LED	Light Emitting Diode
LOGIC	Negative Logic Convention (Ground True) State
LSB	Least Significant Byte
Lsb	Least Significant Bit
MB	Megabyte
MSB	Most Significant Byte
Msb	Most Significant Bit
m	Milli
MPU	Microprocessor Unit
MIL	Military Specifications
MODEM	Modulation/Demodulation Unit
Module	A functional unit that plugs into an assembly
Motherboard	A printed circuit connector interface board with no active or passive components
MOS	Metal-Oxide Semiconductor
MOV	Metal-Oxide Varistor
MS	Military Standards

M/170	Program Module/Model 170 Controller Unit Connector
M/170E	Model 170E Auxiliary Board Connector
N.C.	Normally closed contact
N.O.	Normally open contact
NA	Presently Not Assigned. Cannot be used by the manufacturer for other purposes
NEMA	National Electrical Manufacturer's Association
NETA	National Electrical Testing Association, Inc.
n	nano
NLSB	Next Least Significant Byte
Nlsb	Next Least Significant Bit
NMSB	Next Most Significant Byte
Nmsb	Next Most Significant Bit
NTCIP	National Transportation Communication for ITS Protocol
PCB	Printed Circuit Board
PDA	Power Distribution Assembly
PLA/PAL	Programmable Array Logic Device
PMPP	Point-to-Multi-Point Protocol
ppm	Parts per million
PPP	Point-to-Point Protocol
PWM	Pulse Width Modulation
RAM	Random Access Memory
RDR	ACIA Receiver Data Register
RF	Radio Frequency
RMS	Root-Mean-Square
ROM	Read Only Memory Device
RTC	Model 170E Controller Unit Real Time Clock. This circuitry provides a 170E CPU IRQ Interrupt pulse clocked off of the local power company's line frequency every 16.67 ms.
RTCA	Real Time Clock Adjuster Circuitry
RTS	Request to Send
RXD	Receive Data
R/W	Model 170E Controller Unit Read/Write Control Line
SCI	Serial Communications Interface
SDLC	Synchronous Data Link Control

S	Logic State
S	second
SS	Second Source. Produced by more than one manufacturer
Shunt	A means of connecting/disconnecting two conductive points on a solderless PCB post heater.
SR	ACIA Status Register
SRAM	Static Random Access Memory Device
SW	Switch
TB	Terminal Block
TDR	ACIA Transmit Data Register
TIA	Telecommunications Industry Association
TOD	Time Of Day Clock
Triac	Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit
TTL	Transistor-Transistor Logic
TSD	Thumb Screw Device. A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No. 2 shall be flat black.) TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal. TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal. TSD No.3 - M3 SOUTHCO #47-81-181-10 or equal.
TXC	Transmit Clock
TXCI	Transmit Clock Input
TXCO	Transmit Clock Output
TXD	Transmit Data
µ	Micro
UL	Underwriter's Laboratories, Inc.
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VMA	Valid Memory Address
VME	Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
VMS	Variable Message Sign
X	Number Value
XX	Manufacturer's Option
WDT	Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and react

CHAPTER 1-SECTION 2
GENERAL

1.2.1 Chapter Conflict

In case of Chapter Conflict, the individual Chapter shall govern over Chapter 1.

1.2.2 Furnished Equipment

All furnished Equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

1.2.3 Interchangeability

The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

ASSEMBLIES	ASSOCIATED DEVICES
Output File #1 & #2	Model 200 Switch Pack Model 210 Monitor Unit Model 430 Heavy Duty Relay
Input File	Models 222, 224, & 232E Detectors Models 242 & 252 Isolators
PDA #2	Model 204 Flasher Unit Model 206 Power Supply Module
PDA #3	Model 200 Switch Pack Model 206 Power Supply Module Model 208 Monitor Unit Model 430 Heavy Duty Relay
PDA #4	Model 206 Power Supply CMS Isolation Module
Model 170E Controller Unit	Cabinet Models 332, 334 & 336 Model 400 MODEM Model 412C Program Module
Model 2070 Controller Unit	Cabinet Models 332, 334, 336 & ITS Model 2070-1 CPU Module Model 2070-2 Field I/O Module Model 2070-3 Front Panel Assembly Model 2070-4 Power Supply Model 2070-5 VME Cage Assembly Model 2070-6 Serial Comm Module Model 2070-7 Serial Comm Module
Input Assembly	Model 222, 222E, 232E & 224 Sensor Unit Model 242 and 252 Isolator Unit Model 218 Serial Interface Unit (SIU)

Output Assembly	Model 200 Switch Pack Unit Model 205 Transfer Relay Unit Model 214 Auxiliary Monitor Unit Model 218 SIU Unit
PDA ITS	2 Model 204 Flasher Units Model 212 Cabinet Monitor Unit Model 216-12 & 216-24 Power Supply Units
Model 2070-N1 Controller Unit	Model 2070 Controller Unit Model 2070-8 NEMA Module Model 2070-2B Field I/O Module Model 2070-4N Field I/O Module
Model 2070-N2 Controller Unit	Model 2070 Controller Unit Model 2070-2N Field I/O Module Model 2070-4N Power Supply Module
Pixel Driver Assembly	Pixel Driver Module

1.2.4 Documentation

1.2.4.1 Manual

Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 8.5 in by 11 in paper, with the exception that schematics, layouts, parts lists and plan details may be on 11 in by 17 in sheets, with each sheet neatly folded to 8.5 in by 11 in size. Manual text font shall be ARIAL BOLD, size 12. Text characters shall be no more than 10 characters per 1 in and 7 lines per 1 in, with the exception of schematic text, which shall be no more than 18 characters per 1 in and 11 lines per 1 in.

1.2.4.2 Parts Listed

The State of California title, device name, date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals. The manual shall be separated into two volumes; volume one shall be labeled as Operating Manual and volume two shall be label as Electrical/Mechanical Drawings.

Volume one of the Manual shall include a table of contents and items 2 to 9 and Volume two shall include a table of contents and items 10 to 12 in order as listed:

Item #	Section #	Description
1	N/A	Table of Contents
2	1	Glossary
3	2	General Description
4	3	General Characteristics
5	4	Installation
6	5	Adjustments

7	**6**	Theory of Operation a. Systems Description (include block diagram). b. Detailed Description of Circuit Operation.
8	**7**	Maintenance a. Preventive Maintenance. b. Trouble Analysis. c. Trouble Shooting Sequence Chart. d. Wave Forms. e. Voltage Measurements. f. Alignment Procedures.
9	**8**	Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).
10	**9**	Electrical Interconnection Details & Drawings.
11	**10**	Schematic and Logic Diagram.
12	**11**	Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.

1.2.4.3 Cabinet Manuals

Manuals and Wiring Diagram Sheets for the Cabinet shall be furnished in a weatherproof plastic pouch placed in the cabinet. Cabinet Wiring Diagrams shall be on non-fading, minimum 22-inch x 34-inch sheets.

1.2.4.4 Draft

A preliminary Draft of the Manual shall be submitted to the Engineer for approval prior to final printing.

1.2.5 Packaging

Each item delivered shall be individually packed in its own shipping container. When loose styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the styrofoam.

1.2.6 Delivery

Each item delivered for testing shall be complete, including manuals, and ready for testing.

1.2.7 Metal Edges

All sharp edges and corners shall be rounded and free of any burrs.

1.2.7.1 Aluminum

Aluminum sheets shall be Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

1.2.7.2 Stainless Steel

Stainless Steel Sheets shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

1.2.7.3 Cold Rolled Steel

Cold Rolled Steel Sheets, Rods, Bars and Extruded shall be Type 1018/1020.

1.2.7.3.1 Plating

All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class l or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

1.2.8 Mechanical Hardware

All Hardware bolts, nuts, washers, screws, hinges and hinge pins shall be stainless steel unless otherwise specified.

1.2.9 Electrical Isolation

Within the circuit of any device, module, or PCB, Electrical Isolation shall be provided between DC logic ground, equipment ground and the AC- (Neutral) conductor. They shall be electrically isolated from each other by 500 MΩ, minimum, when tested at the input terminals with 100 Volts DC.

1.2.10 Daughter Boards

Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with four spacers / metal screws depending on the area supported. Connectors shall be either Flat Cable or PCB Headers. Components are allowed to be mounted under the daughter board.

CHAPTER 1-SECTION 3
COMPONENTS

1.3.1 General

All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

1.3.1.1 Special Design

When a component is of such Special Design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

1.3.1.2 Electronic Circuit

The Electronic Circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

1.3.2 Electronic Components

1.3.2.1 Socket Mounted

NO device shall be Socket Mounted unless specifically called out or requested and approved at Qualified Product List Submittal.

1.3.2.2 Rated Power

NO component shall be operated above 80% of its maximum Rated Voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

1.3.2.3 Manufactured Date

NO component shall be provided where the Manufactured Date is 3 years older than the contract award date. The design life of all components, operating continuously (24 hours a day, 365 days per year) in their circuit application, shall be 10 years or longer.

1.3.2.4 Encapsulation

Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators, transistor arrays and termination networks. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

1.3.2.5 Contractor

The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

1.3.2.6 Temperature Rating

All components used shall be designed for use over the full temperature range specified. The component data sheets shall be the only accepted form of validation of the temperature range. Testing and/or screening of commercial grade components is not permitted.

1.3.3 Capacitors

The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150% except for Supercaps which shall be 110%. Supercaps are capacitors rated less than 10 working Volts DC with capacitance values greater than or equal to 1.0F. Capacitor encasements shall be resistant to cracking, peeling and discoloration. With the exemption of Surface Mount Capacitors, all capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.

1.3.4 Potentiometers

Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements. Potentiometers with ratings less than 1 Watt shall be used only for trimmer type function. The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

1.3.5 Resistors

Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications MIL-R-11F or MIL-R-22684. All resistors shall be insulated and shall be marked, except for surface mount, with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. The value of the resistors shall not vary by more than 5% between -34.6^{0}F and 165.2^{0}F. Check this out, are the units correct?.

1.3.5.1 Thermal

Special Ventilation or Heat Sinking shall be provided for all 2-watt or greater resistors. They shall be insulated from the PCB.

1.3.6 Semiconductor-Devices

1.3.6.1 Solid State

All Solid State devices, except LED's, shall be of the silicon type.

1.3.6.2 Transistors / IC / Diodes

All Transistors, Integrated Circuits, and Diodes shall be a standard type listed by EIA. With exemption of Surface Mount Components, Transistors, Integrated Circuits and Diodes shall be clearly identifiable.

1.3.6.3 Metal Oxide Semi-Conductor

All Metal Oxide Semi-Conductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

1.3.6.4 Device Pin 1

Device Pin "1" locations shall be properly marked on the PCB adjacent to the pin.

1.3.7 Transformers / Inductors

With the exemption of Surface Mount Components, all power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color coded with an approved EIA color code or identified in a manner to facilitate proper installation.

1.3.8 Triacs

Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.

1.3.9 Circuit Breakers

Circuit Breaker shall be UL 489 approved. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the Amperes rating shall be marked and visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from 0.4 ^{0}F to 122 ^{0}F. The minimum Interrupting Capacity shall be 5,000 Amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 Amperes and above, the minimum interrupting capacity shall be 10,000 Amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carling switch Time Delay Curve #24 or equal).

1.3.10 Fuses

All Fuses shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the chassis, PCB or beside the holder. Fuses shall be easily accessible and removable without use of tools.

1.3.11 Switches

2.6.1 Dual-Inline-Package-(DIP)

Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 mA, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 mA, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal). The DIP shall have recessed switches to prevent accidental switching.

2.6.2 5 VDC Logic Switch

5 VDC Logic rating shall be 0.4VA @ 20VAC or DC with contact material of gold over nickel plating or copper alloy. The switch shall be rated for a minimum of 40,000 operations.

2.6.3 12 -24 VDC Logic/Control Switches

12-24 VDC control switch contacts shall be rated for a minimum of five-Amperes resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

2.6.4 Power Rating

The switch contacts shall be rated for a minimum of 10 Amperes resistive load at 120 VAC or 28 VDC and shall be silver over brass or equal.

1.3.12 Terminal Blocks

The terminal blocks shall be barrier type, rated at 20 Amperes and 600 VAC RMS minimum. The terminal screws shall be 0.313 in minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

1.3.13 Wiring / Cabling / Harnesses

1.3.13.1 Harnesses

Harnesses shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize cross talk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements. Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.

1.3.13.2 AC Wiring

Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

1.3.13.3 Cabling

Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

1.3.13.4 Labeling

All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

1.3.13.5 Conforming

All conductors shall conform to MIL-W-16878E/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

1.3.13.6 Conductor Color

Conductor Color identification shall be as follows:

AC - (Neutral) circuits	White.
Equip. Ground	Solid green or continuous green color with 1 or more yellow stripes.
DC logic ground	Solid white or continuous white with a red stripe.
AC + (Line) circuits	Solid black or continuous black with colored stripe.
DC logic ungrounded or signal	Any color not specified.

1.3.14 Indicators / Displays

All indicators and character displays shall be readily visible at a radius of up to 4 ft within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

1.3.14.1 Indicators

All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and visibly illuminated when on. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15 degrees minimum shall be provided for Models 208, 210, 212, 222, 232, 242 and 252, as well as a clearance of 30 degrees minimum for Models 200, 204 and 206.

1.3.14.2 Character Displays

Liquid Crystal Displays (LCD) shall operate at temperatures of -4 ^{0}F to 158 ^{0}F.

1.3.15 Connectors

1.3.15.1 Keyed

All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

1.3.15.2 Type T

The Type **T** connector shall be a single row, 10 position, feed through terminal block. The terminal block shall be a barrier type with 6-32, 0.25 in or longer, nickel plated brass binder head screws. Each terminal shall be permanently identified as to its function.

1.3.15.3 Plastic Circular / M Type

Plastic Circular and M Type connectors - Pin and socket contacts for connectors shall be beryllium copper construction sub-plated with 0.00005 in nickel and plated with 0.0000299 in gold. Pin diameter shall be 0.061811 in. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

1.3.15.4 Edge / PCB

Card Edge and Two-Piece PCB Connectors

1.3.15.4.1 PCB Edge

PCB Edge connectors shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

Operating Voltage:	600 VAC (RMS)
Current Rating:	5.0 Amperes
Insulation Material:	Diallyl Phthalate or Thermoplastic
Insulation Resistance:	5,000 MΩ
Contact Material:	Copper alloy plated with 0.00005 in of nickel and 0.000015 in of gold
Contact Resistance:	0.006 Ohm maximum

1.3.15.4.2 Two Piece PCB

The Two-Piece PCB connector shall meet or exceed the DIN 41612.

1.3.15.4.3 PCB 22/44

The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 0.156 in contact centers.

1.3.15.4.4 PCB 28/56

The PCB 28/56 Connector shall have 28 independent contacts per side, dual sided with 0.156 in contact centers.

1.3.15.4.5 PCB 36/72

The PCB 36/72 Connector shall have 36 independent contacts per side, dual sided with 0.100 in contact centers.

1.3.15.4.6 PCB 43/86

The PCB 43/86 Connector shall have 43 independent contacts per side, dual sided with 0.100 in contact centers.

1.3.15.5 Wire Terminal Connectors

Each wire terminal shall be solderless with PVC insulation and a heavy-duty short - locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.

1.3.15.6 Flat Cable Connectors

Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 0.00015 of gold over 0.00005 inches of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 mega Ohms minimum.

1.3.15.7 PCB Header Post Connectors

Each PCB header post shall be 0.00155 in^2 by 0.343 in high; shall be mounted on 0.156 in centers; and shall be tempered hard brass plated with 0.000015 in of gold over 0.00005 in of nickel.

1.3.15.8 PCB Header Socket Connectors

Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 0.00010 in of gold over 0.00005 in of nickel.

1.3.16 Surge Protection Device

A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 µs and fall in 20 µs to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes. It shall have the following ratings:

Impulse Breakdown:	Less than 1,000 Volts in less than 0.1 us at 10 KV/us.
Standby Current:	Less than 1 mA.
Striking Voltage:	Greater than 212 Volts.

CHAPTER 1-SECTION 4
MECHANICAL

1.4.1 Assemblies

All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 0.75 in from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.4.2 PCB Design

No components, traces, brackets or obstructions shall be within 0.125 in of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.4.3 Model Numbers

The manufacturer's model and serial number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the State model number shall be displayed on the front panel in bold type, at least 0.25 in high.

1.4.4 PCB Connectors

All PCB Connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

1.4.5 Fasteners

All screw type Fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

1.4.6 Workmanship

Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.

1.4.7 Tolerances

The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	+/- 0.0525 in
PCB	+/- 0.010 in
Edge Guides	+/- 0.015 in

CHAPTER 1-SECTION 5
ENGINEERING

1.5.1 Human Engineering

1.5.1.1 Equipment

The Equipment shall be engineered for simplicity, ease of operation and maintenance.

1.5.1.2 Knobs

Knobs shall be a minimum of 0.5 in diameter and a minimum separation of 0.5 in edge to edge.

1.5.1.3 PCB

PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 4.5 lbs or greater than 50 lbs for insertion or removal.

1.5.2 Design Engineering

The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. The design shall take into consideration the protection of personnel from all dangerous voltages.

1.5.3 Generated Noise

No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits

CHAPTER 1-SECTION 6
PRINTED CIRCUIT BOARDS

1.6.1 Design, Fabrication and Mounting

1.6.1.1 Contacts on PCBs

All contacts on PCBs shall be plated with a minimum thickness of 0.00003 in gold over a minimum thickness of 0.000075 in nickel.

1.6.1.2 PCB Design

PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

1.6.1.3 Fabrication

Fabrication of PCBs shall be in compliance with Military Specification MIL-P-13949, except as follows:

1.6.1.3.1 Copper Tracks

NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 in minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 1.0 ounces per square foot with adequate cross section for current to be carried. All copper tracks shall be plated or covered by solder mask to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

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1.6.1.3.2 Military Specification Section 3.3

All PCBs shall conform to Section 3.3 of Military Specification MIL-P-13949G Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better. Class of permissible bow or twist shall be Class C (Table V) or better. Class of permissible warp or twist shall be Class A (Table II) or better.

1.6.1.3.3 Military Specification Section 4.2 through 6.6

Sections 4.2 through 6.6 of Military Specification MIL-P-13949G (inclusive) shall be omitted except as referenced in previous sections of this specification.

1.6.1.4 Mounting

The mounting of parts and assemblies on the PCB shall conform to Military Specification MIL-STD-275E, except as follows:

1.6.1.4.1 Semiconductor Devices

Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 50 ^{o}F or more shall be mounted with spacers, transipads or heat sinks where applicable to prevent contact with the PCB.

1.6.1.4.2 Residual Flux

When completed, all residual flux shall be removed from the PCB.

1.6.1.4.3 Resistance

Except where Surface Mount Components are used, the resistance between any 2 isolated, independent conductor paths shall be at least 100 MΩ when a 500 VDC potential is applied.

1.6.1.4.4 Coated

All PCBs shall be coated with a moisture resistant coating.

1.6.1.4.5 Lateral Separation

Where less than 0.125 in lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.03125 in +/- 0.0156 in thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

1.6.1.5 Connector Edges

Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 0.045 in +/- 0.005 in for 0.1 in spacing and 0.055 in +/- 0.005 in for 0.156 in spacing.

1.6.2 Soldering

1.6.2.1 Hand Soldering

Hand soldering shall comply with Military Specification MIL-STD-2000.

1.6.2.2 Automatic Flow Soldering

Automatic flow soldering shall be a constant speed, conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within +/- 46.4 ^{o}F of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

1.6.2.3 Time-Temperature

If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

1.6.3 Definitions

Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendums.

CHAPTER 1-SECTION 7
QUALITY CONTROL

1.7.1 Components

All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

1.7.2 Subassembly, Unit or Module

Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

1.7.3 Predelivery Repair

1.7.3.1 Defects / Deficiencies

Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

1.7.3.2 PCB Flow Soldering

PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

1.7.3.3 Hand Soldering

Hand soldering is allowed for printed circuit repair.

CHAPTER 1-SECTION 8
ELECTRICAL, ENVIRONMENTAL AND TESTING REQUIREMENTS

1.8.1 General

The requirements called out in these specifications dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to insure compliance.

1.8.2 Certification

These test procedures shall be followed by the Contractor who shall certify that they have conducted inspection and testing in accordance with these specifications.

1.8.3 Inspection

A visual and physical inspection shall include mechanical, dimensional and assembly conformance of all parts of these specifications.

1.8.4 Environmental and Electrical

All components shall be designed for and properly operate within the following limits unless otherwise noted:

Applied Line Voltage: 90 to 135 VAC, note "Power Failure / Restoration" limits
Frequency: 60 (+/-3.0) Hertz
Humidity: 5% to 95%
Ambient Temperature: -34.6 ^{0}F to +165.2 ^{0}F
Shock - Test per Specification MIL-STD-810E Method 516.4.
Vibration - per Specification MIL-STD-810E Method 514.4, equipment class G.

1.8.4.1 Commencement Operation

All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

1.8.4.2 Equipment Compliance

All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in a State accepted cabinet connected to the commercial power lines.

1.8.4.3 Power Line Surge Protection

The power line surge protection shall enable the equipment being tested to withstand (non-destructive) and operate normally following the discharge of a 25 μF capacitor charged to ± 2,000 volts, applied directly across the incoming AC line at a rate of once every 10 seconds for a maximum of 50 occurrences per test. The unit under test will be operated at 68 ^{0}F ± 41 ^{0}F and at 120 (±12) VAC.

1.8.4.4 Operating

The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 68 ^{0}F ±41 ^{0}F and at 120 (+/-12) VAC.

1.8.4.5 Modules

The controller unit communications modules shall be tested resident in a State-accepted controller unit which in turn is housed in the cabinet.

1.8.4.6 CMS System Equipment

CMS system equipment will be tested for compliance as a complete system with power from commercial power lines applied at the CMS CIP Panel.

1.8.4.7 UL Requirements

Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

1.8.4.8 Normal Operation

All equipment shall continue normal operation when subjected to the following:

1.8.4.8.1 Low Temperature Test

With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be lowered from 68 ^{0}F to 34.6 ^{0}F at a rate of not more than 64.4 ^{0}F per hour. The item shall be cycled at -34.6 ^{0}F for a minimum of 5 hours and then returned to 68 ^{0}F at the same rate.

1.8.4.8.2 High Temperature Test

With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be raised from 68 ^{0}F to 165.2 ^{0}F at a rate of not more than 64.4 ^{0}F per hour. The item shall be cycled at 165.2 ^{0}F for 5 hours and then returned to 68 ^{0}F at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.3 Normal Operation

All equipment shall resume normal operation following a period of at least 5 hours at -34.6 ^{0}F and less than 10 percent humidity and at least 5 hours at 165.2 ^{0}F and 22% humidity, when 90 VAC is applied to the incoming AC.

1.8.4.9 Humidity and Ambient Temperature

The relative humidity and ambient temperature values in the following table shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY AT BAROMETRIC PRESSURES (29.92 In. Hg.)

Ambient Temperature/ Dry Bulb (in ^{0}F)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in ^{0}F)
-34.6 to 33.98	10	1.04 to 108.86
33.98 to 114.8	95	108.86
119.84	70	108.86
129.92	50	108.86
140.0	38	108.86
149.72	28	108.86
160.16	21	108.86
165.2	18	108.86

1.8.4.10 Opening and Closing of Contacts

All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

1.8.5 Contractor's Testing Certification

1.8.5.1 QC / Final Test

A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

1.8.5.2 Quality Control Procedure & Test Report

The quality control procedure and test report format shall be supplied to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

Acceptance testing of all supplied components.
Physical and functional testing of all modules and items.
A minimum 100-hour burn-in of all equipment.
Physical and functional testing of all items.

CHAPTER 1-SECTION 9
CONNECTOR DETAILS

Section Notes:

M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 MegaOhms. The contacts shall be secured in the blocks with stainless steel springs.

M Type connector corner guides shall be stainless steel. The guide pins shall be 1.097 inches in length and the guide sockets shall be 0.625 inches in length.

Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated heat stabilized and fire resistant.

CHAPTER 2
MODEL 170E ENHANCED CONTROLLER & ASSOCIATED MODULES SPECIFICATIONS

CHAPTER 2-SECTION 1
GENERAL

2.1.1 System READ Access Time

With Model 412C Module Resident in the Controller Unit, valid data shall be present at the MPU at least 100 ns prior to the end of the machine cycle.

2.1.2 Diagnostic and Acceptance Test (DAT) Program

The DAT-170E Program shall be provided resident on the Model 412C Program Module U1 memory device and on the CPU U6 memory device. A copy of the DAT Programs will be available to the contractor at no charge.

2.1.3 PAL, EPROM, or ROM Devices

If a PAL, EPROM, or ROM device is used in address decoding and timing algorithms, the device code listing together with data sheet(s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the Contractor uses to directly reproduce the device.

2.1.4 System Address Organization

The system address organization of the Model 170E shall consist of two addressing configurations. The Decoder Input shall be furnished jumpered in address configuration 1. The internal module address organization shall be as specified in the appropriate module section.

2.1.4.1 Configurations

The two addressing configurations shall be selectable by use of one post jumper. The jumper shall control the Logic State of one Decoder Circuit Input. The logic line shall be a three-post type with the two logic levels on the outer posts. The following input line state conditions shall cause the Decoder circuit to provide the associated address configurations:

CONFIGURATION	LINE	FUNCTION
1.	+5 VDC	170E / 412C
2.	DC GND	170E INTERNAL / 170

2.1.4.2 Configuration 1-Address Organization

FUNCTION	ADDRESS RANGE	COMMENTS	
CPU SRAM	0000-0FFF		
U4 Memory	1000-3FFF	412C	
Reserved	4000-4FFF		
DTA Minutes	5000	READ	
DTA Reset	5000	WRITE	
INPUT / OUTPUT	5001-5008		
	5009-500A	WRITE	
RESTART State	5004	BIT 1 READ	
DTA Seconds	500F	READ	
Reserve	5009-500E	READ	
	500B-500F	WRITE	
	5010-5FFE		
CPU STATUS	5FFF	READ	Bit 1 - ACIA #1 IRQ
			Bit 2 - ACIA #2 IRQ
			Bit 3 - ACIA #3 IRQ
			Bit 4 - ACIA #4 IRQ
			Bit 5 - Reserved
			Bit 6 – Address Configuration
			Bit 7 - DTA Timeout
			Bit 8 - RTC IRQ
RTC Reset	5FFF	WRITE	
ACIA #1	6000	WRITE CR, READ SR	
ACIA #1	6001	WRITE TDR, READ RDR	
ACIA #2	6002	WRITE CR, READ SR	
ACIA #2	6003	WRITE TDR, READ RDR	
ACIA #3	6004	WRITE CR, READ SR	
ACIA #3	6005	WRITE TDR, READ RDR	
ACIA #4	6006	WRITE CR, READ SR	
ACIA #4	6007	WRITE TDR, READ RDR	
Reserve	6008-600F		
CPU SRAM	6010-6FFF		

Program Module

Memory Write Protect	7000	WRITE
I.D. Feature	7000	READ
I.D. Location	7001	READ
	7001	WRITE Reserve
Reserve	7002-7009	
	700B-700E	WRITE
	700F	READ
RTCA Valid/Reset	700A	
RTCA Counters 1 to 4	700B-700E	READ
U3 Memory	7010-7FFF	
U1 & U2 Memory	8000- FFFF	

Note -- Address locations noted as "Reserve" are assignable by the Agency only and shall not be used. CPU STATUS Bit 6: "0" equals Address Configuration 1 and "1" equals Address Configuration 2.

2.1.4.3 Configurations 2-Address Organization

Configuration 2 Address Organization - This configuration provides all Model 412C Program Module features internal to the controller unit. The address organization is the same as CONFIGURATION 1 with the following exceptions:

CPU SRAM	0000-3FFF	U3 & U4 Memory internal
	6010-6FFF	
	7010-7FFF	
U6 EPROM	8000-FFFF	U1 & U2 Memory internal

2.1.5 Memory Devices

Each memory device shall stabilize to normal operation within 10 ms following Power Restoration and shall be in Standby until addressed. Each device shall have the following maximum power drain at +5 VDC in its various states:

MEMORY	ACTIVE	STANDBY	POWERDOWN
EPROM	100 ma	40 ma	-
SRAM	85 ma	20 ma	100 µa (non-internal power)

2.1.6 Prom Memory Sockets

PROM Memory Sockets shall be a 28 Pin AMP Diplomate LF #641894-2, or equal. The MPU, ACIA and other memory sockets shall be an AUGAT #500/800 series AG10DPC or equal. Each socket number shall be permanently marked on the PCB adjacent to its Pin 1. Should the "... or equal MPU" Pin / Package be other than the 40 pin package, the MPU socket used shall match the above specified socket features.

CHAPTER 2-SECTION 2
MODEL 170E CONTROLLER UNIT

2.2.1 Unit Composition

2.2.1.1 170E Controller Consisting

The Model 170E Controller Unit shall consist of the following:

- Central Processing Unit (CPU)
- Input / Output Interface
- Unit Chassis
- M170E Auxiliary Board
- Model 412C Program Module
- Unit Power Supply with external power connection
- Unit Standby Power
- Front Panel Assembly
- Internal System Interface
- Connectors C1S, C2S, C20S, C30S, C40S, and T-1
- Communications System Interface

2.2.1.2 Configuration

The 170E shall be delivered pinned for Configuration 1 Addressing.

2.2.1.3 Composition Weight

The composition weight shall not exceed 25 lbs.

2.2.2 Central Processing Unit (CPU)

2.2.2.1 Micro Processing Unit (MPU)

The CPU shall be provided with an MPU and shall properly execute object programs developed to operate on the MPU. The MPU interrupt requirements shall be as follows:

2.2.2.1.1 Non-Maskable Interrupt (NMI)

The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the MPU NMI line to immediately go LOW. The line shall be held LOW until the RES goes LOW to prevent multiple NMI issuance.

2.2.2.1.2 Reset Interrupt (RES)

The RES is exclusively assigned to Power Restoration and MPU Startup. The RES line shall go LOW 3 (±1) ms following the NMI going LOW. The line shall remain LOW until 150 (±75) ms after Power Restoration.

2.2.2.1.3 Interrupt Request (IRQ)

The IRQ Line shall be jointly used by the RTC and Four ACIAs to initiate IRQ to the MPU.

2.2.2.1.3.1 Real Time Clock (RTC)

Real Time Clock circuitry shall be provided to trigger an interrupt to the MPU on the IRQ line once every 1/60 of a second during the 270 degree to 330 degree portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency. The RTC shall be READ at Bit 8, Address 5FFF (STATUS) and reset by a WRITE to Address 5FFF.

2.2.2.1.3.2 ACIA

Four ACIAs shall be provided, each capable of receiving and transmitting up to eight-bits of parallel data from the MPU for serial data communications. The ACIA shall have 4 registers which are addressable by the MPU. The MPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR), and writing in the Transmit Data Register (TDR) and in the Control Register (CR).

2.2.2.1.3.3 Jumpers

Each ACIA shall be provided with a 2 post type jumper between its IRQ output and the MPU IRQ input. The 170E shall be delivered with these jumpers installed.

2.2.2.2 CPU Clock Timing

The CPU clock circuitry shall be provided to generate the MPU clock timing. The clock circuitry and the MPU shall provide two selectable MPU machine cycle times of 0.651 and 1.302 (±0.0015) µs. The machine cycle time selection shall be by Post Jumper (Three Post Type) with jumper in for 1.302 µs. The CPU clock circuitry shall be located no further than 2 in from the MPU clock pin inputs.

2.2.2.3 SRAM Memory

SRAM Memory, DALLAS 1235Y or equal, shall be provided.

2.2.1.4 AN EPROM Memory

AN EPROM Memory, ST Microelectronics M27C256B or equal, shall be provided in socket U6.

2.2.2.4 Restart Timer

A Restart Timer Circuitry shall be provided to react to the duration of power outage. The Restart Timer output is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (±0.25) seconds, its output state shall go to LOW and remain in that state for 50 (±24) ms after the RES line goes HIGH. If power is restored prior to the timer timing out, the output shall remain HIGH and the timer shall be reset to “0”.

2.2.3 DownTime Accumulator (DTA)

2.2.3.1 Power Failure and Restoration

A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon NMI line going LOW and continue counting until the RES line goes HIGH following Power Restoration.

2.2.3.2 Binary Registers

The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ±1 second over the 255-minute range. The DTA shall stop counting when the Minutes register equals 255 decimal. Both DTA registers shall reset to 0 by a WRITE to Address 5000. The DTA shall READ Minutes at Address 5000 and Seconds at Address 500F. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and reset the other register to "0".

2.2.4 Current Drain

Total Current Drain for DTA AND Restart Timer Circuitry (powerdown mode) shall not exceed 400 µA at 5 VDC, 95^0F while timing and 100 µa at 5 VDC when timeout is latches.

2.2.5 Input / Output Interface

2.2.5.1 Ground True Logic

Input / Output Interface shall utilize a ground true logic. The transfer of data between interface and working registers within the MPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of the MPU read / write command at the time the given address is valid.

2.2.5.2 Output Interface

The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

2.2.5.3 Input Interface

The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC, shall be turned OFF (false) when the input current is less than 100 μa or the input voltage exceeds 8.5 VDC, shall pull up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

2.2.6 Unit Chassis

The controller unit shall be housed in a compact, portable metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 19-inch rack. The enclosure shall be designed for convenient removal of PCBs without the use of tools.

2.2.7 Unit Power Supply

2.2.7.1 Power Supply

A power supply shall be provided to produce all DC power necessary to operate the controller unit. In addition, the supply shall provide the following voltages and current:

1. 1000 mA at +12 VDC
2. 300 mA at -12 VDC
3. 500 mA at + 5 VDC
4. 400 mA at- 5 VDC

2.2.7.2 DC Ground

The DC ground shall not be connected to equipment ground.

2.2.7.3 Controller Unit power

Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ±17 ms beyond the NMI line going LOW.

2.2.7.4 Maximum DC Voltage

The maximum DC voltage generated shall not exceed 45 volts.

2.2.7.5 Power Supply

The Power Supply shall be so designed that no further filtering regulation is needed for the required DC voltages.

2.2.7.6 Radio Frequency Suppressors

Radio frequency suppressors shall be provided on the AC+ and AC- power lines. The part shall be COR COM 3VS1 or equal.

2.2.8 Unit Standby Power

2.2.8.1 Standby Power Supply

A standby power supply shall be provided to retain power (minimum of 72 hrs) to the CPU Restart Timer, DTA and Internal RTCA during power failure in the controller unit. The supply shall consist of holdup Capacitors, capacitor charging circuitry and power sense / transfer circuitry.

2.2.8.2 Power Sense / Transfer Circuitry

The power sense / transfer circuitry shall sense power loss and transfer battery power immediately to the required circuits. The transfer circuitry shall isolate the capacitors by transistor or relay until power loss transfer. The circuitry shall sense power restoration and transfer back to the normal isolation mode.

2.2.8.3 Charging Circuit

A charging circuit which shall, under normal operating conditions, fully charge and float the standby capacitors consistent with manufacturer's recommendations.

2.2.9 Front Panel Assembly

2.2.9.1 Fastening / Removing

The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

2.2.9.2 Connection

The front panel shall be electrically connected by means of Connector C3. The front panel shall be connected to equipment ground through Connector C3.

2.2.9.3 Character Displays

The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 0.4 in high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the MPU through the output interface to the display shall result in the display of each character in its non-inverted state.

2.2.9.4 Indicators

The front panel shall be provided with 10 LED CALL / ACTIVE indicators.

2.2.9.5 Keyboard

A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MPU shall result in each character being received in its non-inverted state. The character shall consist of 4 bits of binary data, while the character control shall consist of 1 bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 0.075 in^2 and shall be mounted on a minimum of 0.5 in centers; shall have an actuation force between 0.0001102 lbs and 0.0002205 lbs and shall provide a positive tactical indication of contact. Key contacts shall have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact opening.

2.2.9.6 Toggle LOGIC Switch

The front panel shall be provided with a toggle LOGIC switch to enable the stop timing function and shall be labeled "STOP TIMING".

2.2.9.7 Toggle CONTROL Switch and Fuse

An ON-OFF toggle CONTROL switch and fuse shall be provided for AC power. The switch and fuse shall protrude through the front panel, but shall remain with the controller unit chassis when the front panel is removed. The fuse shall be a 3AG Slow Blow type, rated at either 1 or 2 Amperes, dependent upon the controller unit power requirements.

2.2.9.8 Framework

The front panel, under the legend "OPERATING INSTRUCTIONS", shall include a framework to retain a card, 4 in wide by 6 in high by 0.063 in thick.

2.2.10 Internal System Interface

2.2.10.1 Connector Spacing

PCB to PCB Connector spacing shall be a minimum of 1 in. Continuous nylon card guides (permanent locking type) shall be provided for the modules and all internal PCBs.

2.2.10.2 22/44S & 36/72S PCB Connectors

Two PCB 22/44S Connectors shall be provided for the MODEM Modules MC1 and MC2, and two PCB 36/72S Connectors shall be provided for the M170 Connector / Program Module and the M170 Connector / M170E Auxiliary Board.

2.2.10.3 Depth Placement

The depth placement of the vertical M/170 Connector shall be such that the Program Module Front Panel shall be flush with the Model 170E Controller Unit Front Panel when the module is connected.

2.2.11 Data and Address Bus Requirements

2.2.11.1 Data Bus Buffers and Drivers

All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 ns.

2.2.11.2 Address Bus Inputs

All Address Bus Inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 picofarads.

2.2.12 Connector Requirements

2.2.12.1 Connector C1S

Connector C1S shall be mounted on the controller unit providing 44 inputs and 56 outputs of control interface to and from external devices or files.

2.2.12.2 400 MODEM and CPU ACIA Connections

The Model 400 MODEM and CPU ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (TYPE T Connector). The control and data transmission lines for ACIA 1 shall be paralleled through C2S and T-1 connectors. ACIA 2 lines shall be routed to C20S Connector, ACIA 3 to C30S, and ACIA 4 to C40S.

2.2.12.3 Signal Lines and Buffer

ACIA 4 RS 232 Signal Lines and Buffered mirrored signals NMI, RES and ROT Shall be internally route to M170 and M170E as noted in Pin Assignments under Section 5 Details.

2.2.13 Communication System Interface

2.2.13.1 Communication Consisting

The communication system shall consist of the CPU, ACIAs, motherboard connectors and lines, MODEM Module Connectors MC1 & MC2 and interfaces between ACIA & MODEM and both MODEM and ACIA to C2S, C20S, C30S, C40S and Connector / T-1 Terminal. The interface between the ACIA and MODEM shall comply with EIA RS-232-C Standards and all functions under T-1, C2, C20S, C30S, and C40S Connectors are referenced to the ACIA. AUDIO IN and AUDIO OUT are referenced to the MODEM. The RTS and TX Data lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12 VDC respectively.

2.2.13.2 Connectors

C20S, C30S, and C40S Connectors shall meet the requirements for the C2S Connector.

2.2.13.3 Frequencies

A minimum of four baud rate generator frequencies, 19.2 kHz, 38.4 kHz, 76.8 kHz and 153.6 kHz shall be provided at the ACIA Rx / Tx Clock Inputs (pins 3 & 4). The frequency selection shall be by post type jumpers. Each ACIA shall have independent baud rate selection with jumpers delivered pinned for 19.2 kHz.

2.2.14 Electrical Requirements

2.2.14.1 Connection

The front panel and chassis shall be connected to equipment ground.

2.2.14.2 Surge Arrestor

A surge arrestor shall be provided between the AC+ and AC- for protection against powerline noise transients. The surge arrestor shall meet the following requirements:

1.	Recurrent peak voltage:	212 Volts
2.	Energy rating maximum:	20 Joules
3.	Power dissipation, average:	0.85 Watt
4.	Peak current for pulses less than 6 us:	2000 Amperes
5.	Standby current:	less than 1 mA

2.2.14.3 Power Resistors / Inductance

Two 0.5 Ohm, 10 watt wire-wound power resistors with a 0.2µH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three surge arrestors rated for 20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68µF capacitor shall be added between AC+ and AC- coming off the 0.5 Ohm resistor going to the surge arrestors.

2.2.14.4 AC Power

The AC power to the controller unit shall be supplied by a 3-conductor cable at least 3 feet in length. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

2.2.14.5 Test Points

Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 0.063 in diameter and 0.19 in high, minimum. The clearance between test points and other components shall be 0.25 in, minimum.

2.2.15 M170E Auxiliary Board

2.2.15.1 M170E Auxiliary Board

The M170E Auxiliary Board shall contain the RTCA Circuitry and the Identification Switches. (See Section 3 for the RTCA circuitry and the Identification Switch requirements.) The RTCA circuitry and the Identification Switches on the M170E Auxiliary Board shall be disabled when a Model 412C is installed. The M170 connector pins 71 and / or 72 shall provide a DC Ground path via the Model 412C Module (pins 69 & 70) to M170E connector (pins 71 & 72). A ground true present shall cause board feature disablement.

2.2.15.2 PCB Dimensions

The M170E Auxiliary Board's PCB dimensions shall meet the Model 400 Modem except for the PCB edge connector dimensions.

2.2.15.3 PCB Connector

The M170E Auxiliary Board's PCB connector shall be a PCB 36 / 72 and shall mate with the M170E connector.

CHAPTER 2-SECTION 3
MODEL 400 MODEM MODULE

2.3.1 Modem

The Modem shall provide two-wire half-duplex and four-wire full-duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN / OUT.

2.3.2 Compliance

The Modem shall be compatible with Bell Standard 202S and comply with the following requirements:

2.3.2.1 Data Rate

Data Rate: 300 to 1200 baud modulations.

2.3.2.2 Modulation

Modulation: Phase coherent frequency shift keying (FSK).

2.3.2.3 Data Format

Data Format: Asynchronous, serial by bit.

2.3.2.4 Line and Signal Requirements

Line and Signal Requirements: Type 3002 voice-grade, unconditioned.

2.3.2.5 Interface

ACIA and Modem Interface: EIA - 232 Standards.

2.3.2.6 Tone Carrier Frequencies

Tone Carrier Frequencies (Transmit & Receive): 1200 Hz (MARK) and 2200 Hz (SPACE) with ±1% tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

2.3.2.7 Transmitting Output Signal Level

Transmitting Output Signal Level: 0, -2, -4, -6 and –8 dB (at 1700 Hz) continuous or switch selectable.

2.3.2.8 Receiver Input Sensitivity

Receiver Input Sensitivity: 0 to –40 dB.

2.3.2.9 Receiver Bandpass Filter

Receiver Bandpass Filter: Shall meet the error rate requirement and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

2.3.2.10 Clear-to-Send (CTS)

Clear-to-Send (CTS) Delay: 12 (±2) ms.

2.3.2.11 Receive Line Signal Detect Time

Receive Line Signal Detect Time: 8 (±2) ms mark frequency.

2.3.2.12 Receive Line Squelch

Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

2.3.2.13 Turn Off Time

Soft Carrier (900 Hz) Turn Off Time: 10 (±2) ms.

2.3.2.14 Modem Recovery Timer

Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

2.3.2.15 Error Rate

Error Rate: Shall not exceed 1 bit in 100,000 bits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

2.3.2.16 Transmit Noise

Transmit Noise: Less than –50 dB across 600 Ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

2.3.3 Modem Power Requirements

The Modem power requirements are as follows:

Input Voltage	Maximum Current Consumption
+12 VDC	75 Milliamperes
-12 VDC	75 Milliamperes

2.3.4 Indicators

Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data.

CHAPTER 2-SECTION 4
MODEL 412C PROGRAM MODULE

2.4.1 General Requirements

2.4.1.1 Prevention
A device shall be provided to prevent the module, when inserted upside down, from making contact with the modules' mating connector within the controller unit.

2.4.1.2 Module PCB Connector
The module PCB Connector shall be provided with electrostatic discharge protection to prevent CMOS device damage.

2.4.1.3 VMA / Phase 2 (E) Clock Signal
The VMA / Phase 2 (E) Clock Signal (M/170 Pin 25) shall not be used in a memory device READ operation.

2.4.1.4 Current Requirements
The total module current requirements shall not exceed 450 mA at +12 VDC and 100 mA at +5 VDC.

2.4.1.5 Program Model 412 Identifier
Address 700E, Bit 8 shall permanently Read as "1". This bit state is used to differentiate between past delivered Model 412/64 modules (Bit 8 decoded "0") and the Model 412C module.

2.4.1.6 Module PCB Connector
The module PCB connector shall be a PCB 36/72P.

2.4.1.7 Module Front Panel
The module front panel shall be connected to Equipment Ground at M170 Pin 34.

2.4.1.8 Addressable Devices
All addressable devices shall be fully decoded.

2.4.1.9 Memory Sockets
All memory sockets shall be a 28 pin AUGAT #528/828 Series AG10DPC or equal.

2.4.2 Feature Requirements

2.4.2.1 Bus Inputs and Outputs

2.4.2.1.1 Data Lines
All data lines shall be tri-state buffered on the module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed, the data output lines shall be disabled into a high impedance state and the data lines shall not source or sink more than 100 µA.

2.4.2.1.2 Addressed Input Lines
All addressed input lines shall load the bus by 1 TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 ns.

2.4.2.2 Memory

2.4.2.2.1 Memory Sockets
Four numbered memory sockets shall be provided and fully decoded using the following method. The module shall be delivered with MEMORY SELECT #3 Configuration designated memory devices (OR EQUAL), address decode and jumpers.

2.4.2.2.2 Device Manufacturer

Device manufacturer is designated as INT-Intel, D-Dallas and HD-Hitachi. The sockets shall be decoded by block jumper selection as follows:

	MEMORY SELECT	SOCKET ADDRESS RANGE AND DEVICE			JUMPER PATTERN		
	U1	U2	U3	U4	1	2	3
1.	E000-FFFF INT2764A	C000-DFFF INT2764A	7010-7FFF DAL1225	1000-4FFF HD6264 OR HD62256	IN	IN	OUT
2.	C000-FFFF INT128A	8000-BFFF NT128A	SAME	SAME	OUT	IN	IN
3.	8000-FFFF	NOT ADRS	SAME	SAME	OUT	OUT	IN
4.	8000-FFFF INT27256A	3000-4FFF DAL1225	SAME	1000-2FFF SAME *	OUT	OUT	OUT

* The pin #26 jumper pattern shall provide either address line 13 for the HD62256 device or tied HIGH for CS2 function in HD6264. Pin 27 shall be assigned to WE function.

2.4.2.2.3 Jumper Positions

Jumper positions for Sockets U2 and U4 shall be provided to convert the sockets from an EPROM socket to a SRAM socket or vice versa. Jumper positions for Sockets U2, U3 and U4 shall be provided to convert the socket from a non-standby power socket to a standby power socket or vice versa. Sockets U2 and U3 shall be jumpered for non-standby power. Socket U4 shall be jumpered for standby power.

2.4.2.2.4 Write Protect Circuit (WPC)

A Write Protect Circuit (WPC) shall be provided to prevent writing to SRAM memory during the Controller Unit MPU RESET Interrupt Line in a LOW State. A WRITE to ADDRESS 7000 shall be decoded and shall activate the WPC to place the R/W in a READ ONLY State. A subsequent WRITE to ADDRESS 7000 shall be decoded and shall deactivate the WPC allowing R/W function. The WPC state shall be brought out to address 700E, Bit 7 ("1" State means "active"). The WPC power drain shall not exceed 40 µA at +5 VDC.

2.4.2.3 Module Power Supply

2.4.2.3.1 Power Supply

A power supply shall be provided onboard the module consisting of a DC Regulation Circuit, Standby Power and all necessary support circuitry.

2.4.2.3.2 DC Regulator Device

A DC Regulator device with its circuitry shall be provided to reduce the +12 VDC to +5 VDC for module use. The Regulator shall have a minimum efficiency of 75% and provide +5 ±0.25 VDC from no load to full load with a maximum of 2% ripple.

2.4.2.3.3 Standby Power

Standby power shall be provided to holdup WPC, SRAM and RTCA circuits during a Model 170 Controller Unit Power Failure. A circuit shall be provided to sense the +12 VDC M/170 power line and switch to standby power when the line falls below +9

VDC. The standby power circuit shall switch off when the power line is greater than +11 VDC. The standby power shall be a standard "AA" cap terminal cell battery rated at a minimum of 1.6 Ampere-hours at 3.7 ±0.2 VDC. All module circuitry and devices shall not exceed a maximum power drain of 2 mA at 3.7 VDC on the Standby Battery.

2.4.2.3.4 Battery

The battery shall be delivered separate from the module. It shall not be used except for test loading check by the Contractor.

2.4.2.3.5 Battery Holder

A battery holder for a “AA” battery shall be provided securely mounted to the back of the front panel. The holder shall have a TAB header type connector attached to the battery's plus cathode mounting terminal.

2.4.2.4 Identification Switch Circuitry

2.4.2.4.1 Switch Packages and Associated Circuitry

Two identification packages 8-position SPST DIP switches and associated circuitry shall be provided. The switch packages shall be decoded at Address 7000 (features) and 7001 (locations). Each package shall have 8 SPST switch positions with each switch associated to a DATA Bit (Switch 1 to Bit 1 and so on). Switch ON shall denote a bit state and shall be read logic "1" by the 170 CPU MPU and Switch OFF shall denote bit state and shall be read logic "0" by the 170 CPU MPU.

2.4.2.4.2 Switch Package

The Switch Package shall be a DIP slide type.

2.4.2.5 Real Time Clock Adjuster (RTCA)

2.4.2.5.1 RTCA Adjusting

A RTCA shall be provided to adjust for missing RTC timing interrupts.

2.4.2.5.2 RTCA Accuracy

The RTCA shall be continuously powered and not affected by a controller unit power failure. RTCA accuracy shall be ±10 ppm at 77 ^{0}F. Integral devices incorporating RTCA features and functions may be used in lieu of individual components. The RTCA current drain shall not exceed 1.5 mA at +3.7 VDC.

2.4.2.5.3 Pulse Generator (PG)

The RTCA shall include a free running 60 Hz Pulse Generator (PG), a 24 bit binary counter counting 60 Hz pulses, 4 eight-bit buffer ports and port decode / PG interrupt logic. The PG shall trigger binary counter to increment on every input pulse, counting continuously until reset to 0 by its Reset Line. Bits 21, 22, 23 and 24 in an all "1"'s state shall cause that PG to be disabled (Binary Counter Bit 1 is the least significant bit).

2.4.2.5.4 Counter Bits

The counter bits shall be continuously read out to 4 eight-bit buffer ports. The ports shall be addressed and bits assigned as follows:

CPU ADDRESS	PORT BITS	COUNTER BITS	COMMENTS

700A	This address shall normally READ (decode) "55 HEX". If the standby power supply fails or is removed, it shall decode "54 HEX". A WRITE to this address will RESET the RTCA Binary Counter.		
700B	1-6	1-6	READ Only
700C	1-6	7-12	READ Only
700D	1-6	13-18	READ Only
700E	1-6	19-24	READ Only

2.4.2.5.5 LOGIC Switch

A SPST finger throw LOGIC switch shall be provided on the board to activate/deactivate standby power to the RTCA Circuitry. With the switch in the deactivated state the RTCA Circuitry shall present NO power drain to the standby power supply.

CHAPTER 2-SECTION 5
MODEL 400N ETHERNET MODULE

2.5.1 Model 400N Ethernet Module

The Model 400N Ethernet Module shall provide an EIA-232 Asynchronous communications channel. The Model 400N Ethernet Module shall be a 170 plug-in module with EIA-232 activity LEDs on the front edge. The Network Model 400N Ethernet Module shall communicate over standard IEEE 802.3 networks using both TCP (point-to-point) and UDP (point-to-multipoint) protocols.

2.5.2 Mechanical/Electrical Requirements

The Model 400N Ethernet Module shall be dimensionally and electrically designed to fit in a single slot of a standard 170 controller. All components shall be protected from physical damage by a metal cover.
All EIA-232 LED Indicators shall be on the Front Panel.

The Model 400N Ethernet Module shall be provided with LED indicators for 10/100 and Half/Full Duplex Network Communications.

The Main Data Port shall be a 170 male 44 pin edge connector (PCB 22/44) located at the rear. The User Serial port shall be a DB9 Female connector accessible from the front. The Network port shall be a RJ45 modular jack connector accessible from the front. DIP switches shall be externally accessible. The Model 400N Ethernet Module shall be powered directly from the Model 170 Controller's Edge Connector (PCB 22/44).

2.5.3 Functional Requirements.

The Model 400N Ethernet Module shall interface to the 170 controller using controller's Main Port EIA-232.

The Main and User Serial Ports shall operate EIA-232 Asynchronous communications and shall support data rates of 1.2, 2.4, 9.6, 19.2, 38.4, 57.5 and 115.2Kbps.
The Model 400N Ethernet Module Network Interface shall meet IEEE 802.3 and ANSI 8802-3 Standards and support 10/100 Mbps.

.
The Auxiliary Port shall be configurable to operate as a DCE or DTE.

2.5.4 Network Configuration

The Model 400N Ethernet Module shall support the following features:

TCP and UDP over IP protocols.

Subnet masks for Class A, B, and C networks (see table below):

NETWORK	HOST	Subnet Mask	Example IP Address

CLASS	BITS		
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100
C	8	255.255.255.0	192.168.0.100

Manual or Automatic TCP/IP socket connections configuration.

Telnet access for both configuration and communications.

Dumb Terminal access using a User Serial port for configuring network parameters.

The Ability to adjust packet size and packing algorithm.

The Model 400N Ethernet Module shall be provided with a Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and Serial Settings using a Web Browser.

2.5.5 Data Interfaces

Main Data Port — Model 170 male 44 pin Edge Connector

User Serial Port — EIA-232 (DB9 Female)

Ethernet Data Port — RJ45 EIA 568B Pin Out

2.5.6 Switch Selections for half duplex and full duplex

User Serial Port Directionality — DTE/DCE

Main Port Operation — Enabled / Disabled

DCD — Constant / Switched

RXD Data Flow Control — Constant / Switched

2.5.7 LED Indicators

RTS Green or Red: DTE Request to Send

CTS Green or Red: Network Clear to Send

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

CD Green or Red: Network Data

2.5.8 Power Requirements

170 Module +12 VDC, 3 Watts

2.5.9 Environmental

The Model 400N shall operate within the specification listed in Chapter 1 Section 1.8.4.

CHAPTER 2-SECTION 6
MODEL 400F FIBER OPTICS MODULE

2.6.1 Model 400F Fiber Optics Module

The Model 400F Fiber Optics Module shall provide an RS232 Asynchronous communications channel. The Model 400F Fiber Optics Module (Model 400F) shall be a Plug-in Card style version for the 170 Controller. The Fiber Optic Model 400F shall operate over Single Mode Fiber.

2.6.2 Mechanical/Electrical Requirements

The Plug-in Card Model 400F shall have a protective cover or enclosure.
The Model 400Fs card edge connector shall be fully compatible with the 170 Controller's Modem card slot.
The Auxiliary Data port shall be a RJ45 connector.
All DIP Switches shall be accessed externally without disassembly of the Model 400F.
The Model 400F will be powered direct from the 170 Controller's edge connector.

2.6.3 Fiber Optics Module Requirements

The Model 400F shall meet the Fiber Optics Requirements of the Model 2070-6D Module as specified elsewhere in these specifications.

2.6.4 Electro Optical Requirements

The Model 400F shall meet the Electro Optical Requirements of the Model 2070-6D Module as specified elsewhere in these specifications.

2.6.5 Form Factor

See A2-8 for details

2.6.6 Power Requirements

The Model 400F shall draw less than 500mA on Model 170 ± 12VDC Power Supply.

2.6.7 Environmental

The Model 400F shall operate within the specifications listed in Chapter 1 Section 1.8.4

CHAPTER 2-SECTION 7
MODEL 170E DETAILS

NOTES:

1. Program module' height and width dimensions are maximum.

2. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.

3. All function under connector C2 & the terminal block T-1 are in reference to the MODEM

4. Detail Definitions:

BL	= BLANKING
CC	= CHARACTER CONTROL OR STROBE
CD	= CARRIER DETECT
CH	= CHARACTER
CTS	= CLEAR TO SEND
DP	= DECIMAL POINT
LS	= LEAST SIGNIFICANT
MS	= MOST SIGNIFICANT
NA	= PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
NLS	= NEXT LEAST SIGNIFICANT
NMS	= NEST MOST SIGNIFICANT
P&I	= PHASE AND INTERVAL
RTS	= REQUEST TO SEND

CHAPTER 3
AUXILIARY CABINET SPECIFICATIONS

CHAPTER 3-SECTION 1
GENERAL REQUIREMENTS

3.1.1 Models 200 and 204 General

3.1.1.1 Unit Chassis

The unit chassis shall be made of metal suitable to meet rigid support and environmental requirements. Where electrical isolation is the only requirement, plastic insulation material can be used in lieu of metal.

3.1.1.2 Unit Control Circuitry and Switches

The unit control circuitry and switches shall be readily accessible by the use of a screwdriver or wrench. Only one type of screw head end (Slotted or Phillips) shall be used.

3.1.1.3 Unit Handle

The unit shall be so constructed that no live voltage is exposed. A handle shall be attached to the front panel for insertion or removal from the unit mating connector.

3.1.1.4 Unit Lower Surface

The unit shall be so constructed that its lower surface shall be no more than 2.06 in below the centerline of the connector and no part shall extend more than 0.9 in to the left or 1.1 in to the right of the connector centerline.

3.1.1.5 Edge Guides

Continuous edge guides shall be provided on the unit.

3.1.1.6 Switching

Each switch shall be capable of switching any Current from 0.050 to 10.0 Amperes (AC) load with power factor of 0.85 or higher.

3.1.1.7 Operations

Each switch shall be designed for a minimum of 300 Million operations while switching a tungsten load of 1000 Watts at 158 ^{0}F. Switch isolation between DC input and AC output circuit shall be at least 10,000 meg-Ohms at 2000 VDC.

3.1.1.8 Positions

Each switch shall turn ON within ± 5 degrees of the zero voltage point of the AC sinusoidal line, and shall turn OFF within ± 5 degrees of the zero current point of the alternating current sinusoidal line. After power restoration, the zero voltage turn ON may be within ± 10 degrees of the zero voltage point only during the first half cycle of line voltage during which an input signal is applied. Turn ON and OFF shall be within 8.33 ms following application or removal of the logic signal, respectively.

CHAPTER 3-SECTION 2
MODEL 200 SWITCH PACK UNIT

3.2.1 Switches

The Model 200 Switch Pack Unit shall be a modular plug-in device containing three solid-state switches. Each switch shall open or close a connection between applied power and external load.

3.2.2 Grounds

A Ground True Controller Unit Input (0 to 6 VDC) shall cause the switch to energize and a Ground False (16 VDC or more) shall cause it to de-energize, State transition shall occur between 6 and 16 VDC. The input shall not sink more than 20 ma or be subjected to more than 30 VDC. The input shall have reverse polarity protection.

3.2.3 Maximum Currents

With all switches on, the unit shall not draw more than 60 mA at +16 VDC or more from the +24 VDC cabinet supply.

3.2.4 Rating

Each switch shall have an OFF state dv/dt rating of 100 V/µs or better. Each switch shall be isolated so that line transients or switch failure shall not alter the controller unit.

3.2.5 Unit Front Panel

The unit front panel shall have an indicator on the input to each switch. The indicator shall be labeled or color-coded “Red”-top switch, “Yellow”-middle switch, and “Green”-bottom switch. The middle switch indicator shall be vertically centered on the unit front panel with the other indicators positioned 1 in above and below.

3.2.6 Resistance

The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15K Ohms when the switch is in open state. When the switch is in off state the output current through the load shall not exceed 20 mA peak.

CHAPTER 3-SECTION 3
MODELS 204 - FLASHER UNIT AND
205 – TRANSFER RELAY UNIT

3.3.1 Model 204 Flasher Unit

3.3.1.1 Flasher Unit
The Flasher Unit shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. The unit's function is to alternatively open and close connections between applied power and external load.

3.3.1.2 Internal DC Power
The unit shall generate its own internal DC power from the AC Line.

3.3.1.3 Flashing
The unit shall commence flashing operation when AC power is applied providing 50 to 60 flashes per minute per switch with a 50 % duty cycle.

3.3.1.4 Rating
Each switch shall have an OFF state dv /dt rating of 200 V/µs or better.

3.3.1.5 Indicator
An indicator showing the switch's output state shall be provided. The two indicators shall be centered with 1 in minimum spacing.

3.3.1.6 Operation
Each circuit shall be designed to operate in an open-circuit condition without load for 10 years minimum.

3.3.1.7 Arrestor
A surge arrestor shall be provided between AC (pin 11) and Flasher Output (pins 7 & 8). The arrestor shall meet the following requirements:

Recurrent Peak Voltage	212 Volts
Maximum Energy Rating	50 Joules
Average Power Dissipation	0.85 Watts
Peak I for pulses less than 6 us	2000 Amperes
Standby I	less than 1 mA

3.3.2 Model 205 Transfer Relay Unit

3.3.2.1 Type
The Transfer Relay Unit shall be of electromechanical type, designed for continuous duty:

3.3.2.2 Cover
Each unit shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating, and part number shall be placed on the cover. They shall be durable, permanent and readily visible.

3.3.2.3 Contacts
Each unit shall be provided with DPDT contacts. The contact points shall be of fine silver, silver alloy or a superior alternate material. Contact points and arms shall be capable of switching 20 Amperes or 1 Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitation. The points and arms shall be able to withstand 0.1 DA or 10 Gs, 10 –55 Hz without contact chatter.

3.3.2.4 Relay Coil
The relay coil shall have a power consumption of 2.0 Volt - Ampere maximum.

3.3.2.5 Relay Potential and Rating

Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a one cycle surge rating of 175 Amperes RMS and pickup and drop out within 20 ms.

CHAPTER 3-SECTION 4
MODEL 206 POWER SUPPLY UNIT

3.4.1 Unit Chassis

The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.4.2 Unit Design

The unit shall provide +24 VDC to the cabinet files. The unit shall be of ferro-resonant design. It shall have no active components and conform to the following requirements:

3.4.2.1 Input Protection

Two 0.5 Ohm, 10-watt wire-wound power resistors with a 0.2 μh inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 μf. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.4.2.2 Line and Load Regulation

Line and load regulation shall meet the power supply range for +24 VDC (23.0 to 26 VDC). This includes ripple noise; from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 86 ^{0}F above ambient.

3.4.2.3 Design Voltage

Design Voltage - +24 +/- 0.5 VDC at full load, 86 ^{0}F, 115 VAC incoming after a 30-minute warm-up period.

3.4.2.4 Full Load Current

Full Load Current 5 Amperes each for +24 VDC, minimum.

3.4.2.5 Ripple Noise

Ripple Noise - 2 volts peak-to-peak and 500 mV RMS at full load.

3.4.2.6 Efficiency

Efficiency - 70% minimum.

3.4.2.7 Circuit Capacitors

Circuit capacitors shall be rated for 40 volts minimum.

3.4.3 Front Panel and Terminals

The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

CHAPTER 3-SECTION 5
MODEL 208 MONITOR UNIT

3.5.1 Monitoring

The Model 208 Monitor Unit shall reliably sense and cause a relay output contact (Failed State) when monitoring the following:

1. A Watchdog Timer (WDT) Timeout Condition
2. Cabinet +24 VDC Power Supply below specified threshold

3.5.2 WDT Monitor Requirements

3.5.2.1 WDT Circuitry

WDT Circuitry shall be provided to monitor a controller unit output line state routed to the monitor unit at its assigned pin. The WDT Circuitry shall sense any line state change and the time between the last change. No state change for 1.5 6 ±0.1 seconds shall cause a Failed State. The timer shall reset at each state change in a Non Failed state.

3.5.2.2 Unit Reset / WDT

Only the Unit Reset or a WDT inactive due to the voltage sense shall reset the WDT from a failed state.

3.5.2.3 Failed State

A Failed state caused by the WDT shall illuminate a front panel indicator light labeled "WDT ERROR". The indicator shall remain ON until Unit Reset Issuance.

3.5.2.4 WDT Circuitry

The WDT Circuitry shall sense the incoming VAC Line and when the voltage falls below 98 ± 2 VAC for 50 ± 17 ms shall inhibit the WDT Function. When the WDT Circuitry senses the incoming VAC Line rise above 103 ± 2 VAC for 50 ± 2 ms the WDT shall become active. A hysteresis between the Voltage Inhibit and the Voltage Active Settings shall be a minimum of 3 Volts.

3.5.3 Power Supply Monitor Requirements

3.5.3.1 Monitor Unit

The monitor unit shall sense the Cabinet +24 VDC Power Supply Output Voltage. Voltages sensed at +18 VDC or below for a duration of 500 ms or longer shall cause a Failed state. Voltages sensed at +22 VDC or above shall NOT cause a failed state. Voltages sensed below +22 VDC for a duration of 200 ms or less shall NOT cause a Failed state. All timing and voltages conditions other than those specified above may or may not cause a failed state.

3.5.3.2 Indicator

A Failed state caused by sensing the power supply shall illuminate a front panel indicator light labeled "VDC FAILED". The indicator shall remain ON until Unit Reset.

3.5.3.3 Unit Reset

Only Unit Reset shall reset the power supply sense circuitry from a Failed State.

3.5.4 Failed State Output Circuits

An electro-mechanical relay shall be provided to switch an output circuit during a Failed State. The relay coil shall be energized in a Non Failed State. The relay contacts shall be rated for a minimum of 3 Amperes at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 ms or less.

3.5.5 Monitor Unit Reset

A momentary SPST Control switch labeled “RESET” shall be provided on the unit front panel to reset the monitor unit circuitry to a Non Failed state. The switch shall be so positioned on the front panel that the switch can be operated while gripping the front panel handle.

3.5.6 Provision

The unit shall be provided with provision to drive an external NE2H light through a 56 K Ohm, 1/2 Watt series resistor (resident on unit).

3.5.7 PDA #3 WDT Reset Input

The PDA #3 WDT Reset Input shall not be sensed by the unit.

3.5.8 Output Relay

The output relay Contact for Failed State shall be Open.

CHAPTER 3-SECTION 6
MODEL 210 MONITOR UNIT

3.6.1 Monitor Unit Conditions

The Monitor Unit shall sense the following conditions and cause a FAILED STATE should any of the conditions exist:

1. The cabinet +24 VDC power supply below the voltage threshold.
2. The WDT Timeout Condition.
3. Conflicting field Output Circuit ON Condition.

3.6.2 Requirements

See Chapter 3, Section 5 Model 208 Monitor Unit for requirements on Power Supply Monitoring, Watchdog Timer, Failed State Output Circuits and Monitor Unit Reset.

3.6.3 Conflict Monitoring

The monitor shall sense up to 16 Channels for conflict (32 field outputs of Green and Yellow). The Green and Yellow are Logically OR'd together. The associated cabinet output file assignment or operator selected output switches shall determine channel assignment.

3.6.3.1 Monitored Field Output Voltages

All monitored field output voltages shall be measured as true RMS responsive (up to 3 KHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of 2 cycles. If digital means are used in calculating RMS, a minimum of 2 samples shall be taken per alternation.

3.6.3.2 Sensed Conflicting Field Output Voltages

Sensed conflicting field output voltages 25 VAC or greater for a duration of 500 ms or longer shall cause a Failed state. Sensed conflicting field output voltages between 15 VAC or less OR any voltage having a duration of 200 ms or less shall NOT cause a Failed states.

3.6.3.3 Conflict Monitoring Circuitry

The Conflict Monitoring Circuitry shall be capable of detecting both a positive and negative half-wave failure under the foregoing conditions.

3.6.3.4 Failed State

A Failed state caused by sensing voltage conflicts shall be reset only by the Unit Reset.

3.6.3.5 Indicators

Sixteen indicators shall be provided on the unit front panel to indicate if the channel output is sensed ON. The indicators shall remain ON in a latched state during a Failed state unless unlatched by Unit Reset or a unit loss of power during said Failed state.

3.6.4 Conflict Programming Card

3.6.4.1 PCB Programming Card

A plug-in PCB Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically labeled and laid out for easy identification of the diodes by channel. With diodes in place all output channels being monitored shall be in conflict. When the diode (anode to numerical pins and cathode to alphabetical pins) has been removed the channels shall be defined as non-conflict.

3.6.4.2 Pad / Placement

A pad for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin the yellow inhibit common shall disable sensing the said channel yellow.

3.6.4.3 Connection

The programming card shall intermate with a PCB 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provide a mechanically sound card and connector support including continuous card guides. When the programming card is resident in the unit, the card's front end shall be flushed with the unit's front panel.

3.6.4.4 Pins 16 and T

Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.

3.6.5 Conflicting

A front panel indicator labeled "CONFLICT" shall be provided. The indicator shall illuminate when there is a FAILED state caused by conflicting channels and go off only by Unit Reset Issuance.

3.6.6 Output Relay Contact

The output relay contact for FAILED State shall be "CLOSED".

3.6.7 Second Output Circuit

A second output circuit (STOPTIME controller input) shall be provided to sink a NPN Open Collector Transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50 ma at up to 30 VDC. A blocking diode shall be provided on the transistor output to prevent it from souring power into the controller unit.

3.6.8 LOGIC Toggle Switch

An internal SPST LOGIC toggle switch shall be provided on the Model 210 Monitor Unit to activate the WDT function. When the switch is ON the WDT Circuitry shall be active. The switch shall be mounted on the module PCB in a readily accessible location.

3.6.9 RESET Switch

The Front Panel RESET Switch shall be tied to the External Test Reset Input Line (Pin Z). The External Line shall be optically isolated from internal circuitry

CHAPTER 3-SECTION 11
MONITOR UNITS & POWER SUPPLY DETAILS

CHAPTER 4

CHAPTER 4 SECTION 1
GENREAL REQUIREMENTS

(not applicable)

CHAPTER 5
SPECIFICATIONS DETECTOR SENSOR UNITS, ELEMENTS AND ISOLATORS

CHAPTER 5-SECTION 1
GENERAL REQUIREMENTS

5.1.1 Sensor and Isolator Channels

The sensor and isolator channels shall be operationally independent from each other. Each sensor or isolator channel shall draw no more than 50 mA from the +24 VDC cabinet power supply and shall be insensitive to 700 mVolts RMS ripple on the incoming +24 VDC line.

5.1.2 Front Panel

The sensor unit or isolator front panel shall be provided with the following:

Hand pull to facilitate insertion and removal from the input file.
Control switches and Channel Indicators.
Channel visual indication of detection or incoming signal.

5.1.3 Output

Each sensor or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs. The output shall have a minimum impedance of 2 Mega Ohms when no vehicle is detected.

5.1.4 Valid Channel Input

A valid channel input shall cause a channel Ground True Output to the controller unit of a minimum 100 ms in duration. An onboard two-post shunt jumper shall be provided to disallow this requirement when the jumper is in a OPEN position.

5.1.5 Sensor Unit

The sensor unit or sensing element shall operate and interface successfully with an associate CALTRANS Standard Sensing Unit or Element.

5.1.6 Output Transistor

The output transistor shall switch from OFF to ON state or ON to OFF state in 20 µs or less.

5.1.7 Onboard Protection

Onboard protection shall be provided to enable the sensor unit or isolator to withstand the discharge of a 10 µF capacitor charged to +/- 1000 Volts directly across the input pins with no load present. With a dummy load of 5 Ohms, protection shall enable the sensor unit or isolator to withstand the discharge of a 10 µF capacitor charged to +/- 2000 Volts directly across either the input pins or from either side to equipment ground.

CHAPTER 5-SECTION 2
MODEL 222 & 224 LOOP DETECTOR
SENSOR UNIT REQUIREMENTS

5.2.1 Sensor Unit Channel

The sensor unit channel shall produce an output signal when a vehicle passes over or remains over wire loops embedded in the roadway. The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease in inductance of the circuit measured at the input terminals of the sensor unit. The detector zone shall include all configurations listed in paragraph **5.2.9.1**.

5.2.2 Open Loop

An open loop shall cause the sensor unit channel to output a signal.

5.2.3 Detection

Each sensor unit channel shall be capable of detecting all types of California licensed motor vehicles when connected to the loop configuration/lead-in requirements of 5.2.9.1

5.2.4 Sensor Unit Compliance

The sensor unit shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 50 to 700 μH with a Q-parameter as low as 5 at the sensor unit operating frequency.

5.2.5 Loop Inputs

Loop inputs to each channel shall be transformer isolated.

5.2.6 Switches

Each individual channel shall have a minimum of 4 switch selectable operating frequencies.

5.2.7 Tuning Circuits

The sensor unit channel tuning circuits shall be automatic and shall be so designed that drift caused by environmental changes, or changes in applied power shall not cause an actuation.

5.2.8 Modes Selection Requirements

Each sensor unit channel shall have Pulse and Presence selectable modes.

5.2.8.2 Pulse Mode

5.2.8.1.1 Vehicle Presence

In the Pulse Mode, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 (± 25) ms in duration.

5.2.8.1.2 Detection Zone

Should a vehicle remain in a portion of the detection zone for a period in excess of 2 seconds, the sensor unit channel shall automatically "tune out" the presence of said vehicle. The sensor unit channel shall then be capable of detecting another vehicle entering the same detection zone. The recovery time to full sensitivity between the first vehicle pulse and channel capability to detect another vehicle shall be 3 seconds maximum.

5.2.8.3 Presence Mode

5.2.8.2.1 Duration

In the Presence Mode, the sensor unit channel shall recover to normal sensitivity within 1 second after termination of vehicle presence in the detection zone regardless of the duration of the presence.

5.2.8.2.2 Presence Sensitivity Settings

The channel sensitivity settings shall be provided that detect the presence of a vehicle in the detection zone for a specified time period and inductance change(s). The conditions are as follows:

	Minimum Time Duration	Detector Input Inductance Change
Setting 6	3 Minutes 10 Minutes	0.02% or more 0.06% or more
Setting 2	4 Minutes	1.00% or more

5.2.9 Sensitivity

5.2.9.1 Standard Plans Loop Configurations

California Standard Plan ES-5A & B Loop Configurations. (California Department of Transportation Standard Plans.)

5.2.9.1.1 Single Type-250

Single Type A, B, Q or Round Loop with a 250 ft lead-in cable.

5.2.9.1.2 Single Type-1000

Single Type A, B, Q or Round Loop with a 1000 ft lead-in cable.

5.2.9.1.3 4 Type-Series/Parallel-250

4 Type A, B, or Q Loops connected in series/parallel with a 250 ft lead-in cable.

5.2.9.1.4 4 Type-Series-1000

4 Type A, B, Q or Round Loops connected in series with a 1000 ft lead-in cable.

5.2.9.1.5 Type C-250

One 50 foot Type C Loop with a 250 ft lead-in cable.

5.2.9.2 Sensitivity Settings

Each sensor unit channel shall be equipped with a front panel selectable sensitivity setting(s) in presence and pulse modes to accomplish the following under operational and environmental requirements of this specification.

5.2.9.2.1 Setting 2

Each sensor unit channel shall respond while in setting 2 to a nominal change in inductance between 0.15% to 0.4% (median sensitivity of 0.32%) while connected to the above **5.2.9.1** loop configuration. This setting shall not respond to an inductance change of less than 0.1%

5.2.9.2.2 Setting 6

Each sensor unit channel shall respond while in the setting 6 to an induction of 0.02% while connected to the above **5.2.9.1** loop configuration.

5.2.9.3 Vehicle Detection

The sensor unit channel shall not detect vehicles, moving or stopped, at distances of 3 ft or more from any loop perimeter, in all configurations listed in paragraph **5.2.9.1**

5.2.9.4 Differ

All sensitivity settings shall not differ +/- 40% from the nominal value chosen.

5.2.9.5 Selectable Sensitivity Setting(s)

There shall be a minimum of 7 selectable sensitivity settings including specified sensitivity settings.

SETTING	SENSITIVITY	SETTING	SENSITIVITY
1	0.64%	5	0.04%
2	0.32%	6	0.02%
3	0.16%	7	0.01%
4	0.08%	8	Channel OFF

5.2.10 Response Time

Response time of the sensor unit channel for Sensitivity Setting, 2 shall be less than 5 ± 1 ms. That is, for any decreased inductive change which exceeds its sensitivity threshold, the channel shall output a ground true logic level within 5 ± 1ms. When such change is removed, the output shall become an open circuit within 5 ± 1ms.

5.2.11 Normal Operation

The sensor unit channels shall begin normal operation within 2 seconds after the application of power or after a reset signal of 30 µs.

5.2.12 Lightning Protection

Lightning Protection shall be installed within the sensor unit as defined in the Section 5.1.7 of these specifications.

5.2.13 Tracking Rate

The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.

5.2.14 Tracking Range

5.2.14.1 Inductance

The sensor unit shall be capable of normal operation as the input inductance is changed ± 5.0% from the quiescent tuning point regardless of internal circuit drift.

5.2.14.2 Resistance

The sensor unit shall be capable of normal operation as the input resistance is changed ± 0.5% from the quiescent tuning point regardless of internal circuit drift.

5.2.15 Temperature Change

The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes with the rate of temperature change not exceeding 1°C per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18°C between the inside and outside air shall not affect the proper operation of the sensor unit.

5.2.16 Switch

A switch or switch position shall be provided on the front panel to disable each channel output.

CHAPTER 5-SECTION 3
MAGNETIC DETECTOR REQUIREMENTS

5.3.1 Model 231 Magnetic Detector Sensing Element

5.3.1.1 Sensing Element

Each sensing element shall be designed for ease of installation, repositioning, and removal. The sensing element shall be 2.24 in maximum in diameter, have no sharp edges, and its length not to exceed 18 in. The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a 100 ft lead-in cable. Leakage resistance shall be a minimum of 10 MegaOhms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt water bath after the device has been entirely immersed in the bath for a period of 24 hours at 68 ^{0}F +/- 37.4 ^{0}F. The salt water bath concentrate shall be one fourth ounce of salt per gallon of water.

5.3.1.2 Lead-In

Each sensing element including lead-in shall have a DC resistance of less than 3500 Ohms and an inductance of 20 Henrys +/- 15 %.

5.3.2 Model 232 Two Channel Magnetic Detector Sensing Unit

5.3.2.1 Sensing Channel

When resident in an active cabinet input assembly and attached to one or more Model 231E Sensing Elements resident in conduit under the travel way, the sensing channel shall output a Ground True Output to the Controller Unit when sensing an induced voltage caused by a California Licensed Vehicle passing within 6 ft from an element with a 1000 ft of lead-in cable at all speeds between 3.11 and 80.78 mile per hour. The sensing channel output shall be continuous as long as the vehicle is detected. A digital reading switch with 8 selected step positions for Gain (0 to Full) and a momentary test switch providing a voltage test input shall be furnished for each channel on the front panel.

CHAPTER 5-SECTION 4
MODEL 242 TWO-CHANNEL DC ISOLATOR REQUIREMENTS

5.4.1 Model 242 DC Isolator Channel

The Model 242 DC Isolator Channel shall provide isolation between a VDC input circuit (external electrical switch closure) and the controller unit input. The minimum isolation shall be 1000 MegaOhms and 2,500 VDC measured between the input and the output of the same channel.

5.4.2 Test Switch

Each isolation channel shall have a front panel mounted test switch to simulate valid input. The test switch shall be a single-pole double-throw, three position CONTROL test switch: The position assignment shall be UP – constant ON; MIDDLE – OFF; and DOWN – momentary ON.

5.4.3 Internal Power Supply

The isolator shall have an internal power supply supplying 20 +/- 4 VDC to the field input side of the isolation channels. The isolator shall not draw more than 2.5 watts of AC power. No current shall be drawn from the cabinet power supply. PCB should be two layer design minimum, using plated-thru vias, and Gold Plated Fingers on Both Sides of PCB.

5.4.4 Channel Contact Closure Input

A channel contact closure input of 2 ms or less shall not cause an output (ground true) to the controller. An input of 7 ms or greater shall cause an output to the controller. An input of duration between 2 and 7 ms may or may not cause an output to the controller.

5.4.5 Field Input

Each isolation channel field input shall be turned on (true) when a contact closure causes an input voltage of less than 8 VDC, and shall be turned off (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA nor more than 40 mA to an electrical contact closure or short from the power supply.

CHAPTER 5-SECTION 5
MODEL 252 TWO-CHANNEL AC ISOLATOR

5.5.1 Model 252 Two-Channel AC Isolator

The Model 252 Two-Channel AC Isolator shall contain 2 isolation channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits. The method of isolation shall be based upon a design which provides reliable operation.

5.5.2 Channel Input Voltage "Von"

A channel input voltage "Von" of 80 +/- 5 VAC applied for a minimum duration of 110 ms ± 10 ms shall cause an output (Ground True) to the controller unit.

5.5.3 Channel Input Voltage "Voff"

A channel input voltage "Voff" (Von minus 10 VAC) applied for a minimum duration of 110 ms ± 10ms shall cause an output (Ground False) to the controller unit.

5.5.4 Post Jumper

A two post jumper shall be provided to select inverted output states for Von and Voff. When in CLOSED position (Grounded) Von shall cause a Ground False output. An indicator shall be provided on the front panel labeled 'RR" which shall indicate a Voff input, Ground True output.

5.5.5 Input Impedance

The input impedance of each channel shall be between 6,000 - 15,000 Ohms at 60 Hz.

5.5.6 Minimum Isolation

The minimum isolation shall be 1000 MegaOhms between the input and output terminals at 500 AC applied voltage.

CHAPTER 5 SECTION 6
SENSOR & ISOLATOR DETAILS

	Appendix
5.6.1 Sensor Unit and Isolator	**A5-1**

CHAPTER 6
CABINET SPECIFICATIONS
MODELS 332, 334 & 336

CHAPTER 6-SECTION 1
GENERAL REQUIREMENTS AND
CABINET MODEL COMPOSITION

6.1.1 Composition

Unless otherwise specified the model shall be furnished, ready for operation with the following composition.

6.1.1.1 Model 332A Cabinet

Model 332A Cabinet shall consist of:

Housing 1 B	Output File #1
Mounting Cage 1	C1 Harness #1
Power Distribution Assembly #2	Service Panel #1
Input Files I & J	Input Panel #1

6.1.1.2 Model 334C Cabinet

Model 334C Cabinet shall consist of:

Housing 1 B	PDA Assembly #3
Mounting Cage 1	C1 Harness #2
Input File I	Service Panel #1
Input Panel #3	

6.1.1.3 Model 336A Cabinet

MODEL 336A CABINET shall consist of:

Housing 2	Output File #1
Mounting Cage 2	C1 Harness #3
Power distribution Assembly #2	Service Panel #2
Input File I	Input Panel #4

6.1.1.4 Model 336B Cabinet

Model 336B Cabinet shall consist of:

Housing 2	Output File #2 **
Mounting Cage 2	C1 Harness #3
Power Distribution Assembly #2	Service Panel #2
Input File I	Input Panel #4
Monitor Unit Assembly	

** A C1 Harness #3/Output File #2 Adaptor shall be provided.

6.1.1.5 Assemblies and Files

All assemblies and files shall be mounted on the cage mounting rails per cabinet model detail. Cabinet model interface wiring shall be per specified C1 Harness, detailed wiring lists and required One Line Wiring.

6.1.2 Cabinet Shipping Requirements

The cabinet shall be delivered mounted on a plyboard shipping pallet. The pallet shall be bolted to the cabinet base. The cabinet shall be enclosed in a slipcover cardboard packing shell. The housing doors shall be blocked to prevent movement during transportation.

6.1.3 Cabinet Adaptors

When specified, adaptors shall be provided. The adaptor shall be fabricated of the same material and finish as the cabinet housing.

6.1.4 Stainless Steel

All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

6.1.5 Cage Mounting

A cage mounting clear area for the controller unit shall be provided. The area shall extend 1.5 in front of and 16 in behind the front EIA mounting angles.

6.1.6 Protection

All conductors, terminals and parts which could be hazardous to maintenance personnel shall be protected with suitable insulating material.

CHAPTER 6-SECTION 2
HOUSING REQUIREMENTS

6.2.1 Housing

The housing shall include, but not be limited to, the following:

Enclosure	Police Panel
Doors	Ventilization
Latches/Locks	Gasketing
Hinges and Door Catches	Cage Supports and Mounting

6.2.2 Housing Construction

6.2.2.1 Waterproof

The housing shall be rainproof with the top of the enclosure crowned to prevent standing water. It shall have single front and rear doors, each equipped with a lock.

6.2.2.2 Fabricating

The enclosure, doors, lifting eyes, gasket channels, police panel, and all supports welded to the enclosure and doors shall be fabricated of 0.125 in minimum thickness aluminum sheet. Bolted on supports shall be either the same material and thickness as the enclosure or 0.105 in minimum steel. The side panels and filter shell shall be fabricated of 0.080 in minimum thickness aluminum sheet.

6.2.2.3 Exterior

All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filed to a radius of 0.03125 in minimum. Exterior cabinet welds shall be done by gas Tungston arc TIG process only. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum. Internal cabinet welds shall be done by either gas metal arc MIG or gas Tungston arc TIG Process.

6.2.2.4 Aluminum surfaces

Aluminum surfaces shall conform to the following:

6.2.2.4.1 Anodic Coating

An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning and etching procedure shall be to immerse in inhibited alkaline cleaner at 159.8 ^{0}F for 5 minutes (Oakite 61A, Diversey 909 or equivalent in mix of 6 ounces to 8 ounces per gallon to distilled water). Rinse in cold water. Etch in a sodium solution at 150.8 ^{0}F for 5 minutes 0.5 ounce sodium fluoride plus 5 ounces of sodium hydroxide mix per gallon to distilled water. Rinse in cold water. Desmut in a 50% by volume nitric acid solution at 68 ^{0}F for 2 minutes. Rinse in cold water.

6.2.2.4.2 Conforming

The anodic coating shall conform to MIL-A-8625C (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, Class I Coating except the outer housing surface coating shall have a 0.0007 inch minimum thickness and a 0.952 ounces per square inch minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution of nickel acetate (PH 5.0 to 6.5) for 15 minutes at 210.2 ^{0}F.

6.2.2.5 Enclosure Doorframes

The enclosure doorframes shall be double flanged out on all 4 sides and shall have strikers to hold tension on and form a firm seal between the door gasketing and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 0.156 (+/- 0.08) in.

6.2.2.6 Gasketing

Gasketing shall be provided on all door openings and shall be dust-tight. Gaskets shall be 0.25 inch minimum thickness closed cell neoprene or silicone (BOYD R-10480 or equal) and shall be permanently bonded to the metal. If neoprene is used the mating surface of the gasketing shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A Gasket Top Channel shall be provided to support the top gasket on the door (prevent gasket gravitational fatigue).

6.2.2.7 Cage Bottom Support Mounting Angles

Cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness of either 0.188 in aluminum or 0.105 in steel.

6.2.2.8 Lifting Eyes

The housing shall be provided with 2 lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 0.75 in. Each eye shall be able to support a weight load of 1000 pounds.

6.2.2.9 Exterior Bolt Heads

All exterior bolt heads shall be tamperproof type.

6.2.3 Door Latches & Locks

6.2.3.1 Latching Handles

The latching handles shall have provision for padlocking in the closed position. Each handle shall be 0.75 in minimum diameter stainless steel with a minimum 0.5 in shank. The padlocking attachment shall be placed at 4.0 in from the handle shank center to clear the lock and key. An additional 4.0 in minimum gripping length shall be provided.

6.2.3.2 Latching Mechanism

The latching mechanism shall be a three-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 0.25 in thick by 0.75 in wide, minimum.

6.2.3.3 Locks and Handles

When the door is closed and latched, the door shall be locked. The locks and handles shall be on the right side of the front door and left side of the rear door. The lock and lock support shall be rigidly mounted on the door. In the locked position, the bolt throw shall extend a minimum of 0.25 ± 0.03125 in into the latch Cam area. A seal shall be provided to prevent dust or water entry through the lock opening.

6.2.3.4 Locks

The locks shall be Corbin 2 type, or equal. One key shall be supplied with each lock. The keys shall be removable in the locked position only.

6.2.3.5 Bolts

The locks shall have rectangular, spring-loaded bolts. The bolts shall have a 0.281 in throw and shall be 0.75 in wide by 0.75 in thick (tolerance is ±0.035 in).

6.2.3.6 Center Latch Cam

The center latch cam shall be fabricated of a minimum thickness 0.1875 in steel or aluminum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.

6.2.3.7 Rollers

Rollers shall have a minimum diameter of 0.875 in with nylon wheels and steel ball bearings.

6.2.4 Ventilation

The housing ventilation including intake, exhaust, filtration, fan assembly and environmental control are as follows:

6.2.4.1 Front Door

The front door shall be provided with louvered vents. The louvered vent depth shall be a maximum of 0.25 in. A removable and reusable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 0.25 in to house the filter. The filter resident in its shell shall be held firmly in place with a bottom bracket and a spring loaded upper clamp. No incoming air shall bypass the filter. The bottom filter bracket shall be formed into a waterproof sump with drain holes to the outside housing.

6.2.4.2 Intake and Exhaust Areas

The intake (including filter with shell) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for housing #1 and 26 cubic feet of air per minute for housing #2.

6.2.4.3 Electric Fan

The housing shall be equipped with an electric fan with ball or roller bearings and a capacity of at least 100 cubic feet of free air delivery per minute. The fan shall be mounted within the housing and vented.

6.2.4.4 Temperature Controlling

The fan shall be thermostatically controlled and shall be manually adjustable to turn on between 91.4 ^{0}F and 149 ^{0}F with a differential of not more than 42.8 ^{0}F between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor ampacity. The manual adjustment shall be graded in 50 ^{0}F increment scale.

6.2.4.5 Filter

The filter shall be 16 in wide by 12 in high by 0.875 in thick. The filter shall be an ECO-AIR Products E35S or equal.

6.2.5 Hinges & Door Catches

6.2.5.1 Leave Hinges

Two-bolt per leave hinges shall be provided to bolt the enclosure to the door. Housing 1 shall have 4 hinges and Housing 2 three hinges. Each hinge shall be 3.5 in minimum length and have a fixed pin. The pin ends shall be welded to the hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

6.2.5.2 Front and Rear Doors

Front and rear doors shall be provided with catches to hold the door open at both 90 and 180 ±10 degrees. The catch minimum diameter shall be either 0.375 in for plated steel or aluminum rods or 0.25 in for Stainless steel. The catches shall be capable of holding the door open at 90 degrees in a 60 mph wind acting at an angle perpendicular to the plane of the door.

6.2.6 Police Panel

6.2.6.1 Police Panel Assembly

A police panel assembly shall be provided to allow the police officers limited access to intersection control. The police panel assembly including switches shall not extend into the cabinet more than 1.5 in.

6.2.6.2 Police Panel Door

The police panel door shall be equipped with a lock. The lock shall be keyed for a master police key. One key shall be furnished with each police lock. Each police key shall have a shaft at least 1.75 in length.

6.2.6.3 Toggle Power Switches

The police panel shall contain 2 DPST Toggle Power Switches.

6.2.6.3.1 Model 334

One switch shall be labeled "ON-OFF LIGHTS" and the other "POLICE CONTROL ON-OFF".

6.2.6.3.2 Models 332 and 336

One switch shall be labeled “ON-OFF" and the other "FLASH/AUTOMATIC".

6.2.6.3.3 Front and Back of the Panel

The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

6.2.6.3.4 Panel Assembly

The panel assembly shall have a drain to prevent water collecting within the assembly. The drain shall be channeled to the outside.

CHAPTER 6-SECTION 3
CABINET CAGE REQUIREMENTS

6.3.1 EIA 19-inch Rack Cage

A standard EIA 19-in rack cage shall be installed inside the housing for mounting of the controller unit and cabinet assemblies**.**

6.3.2 EIA Rack Portion

The EIA rack portion of the cage shall consist of 2 pairs of continuous, adjustable equipment mounting angles. The angle nominal thickness shall be either 0.1345 in plated steel or 0.105 Stainless Steel. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angle shall comply with Standard EIA RS-310-D and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.

6.3.3 Clearance

Clearance between rails for mounting assemblies shall be 17.75 in.

6.3.4 Angles

Two steel supporting angles extending from the front to the back rails shall be supplied to support the controller unit. The angles shall be designed to support a minimum of 50 pounds each. The horizontal side of each angle shall be a minimum of 3 in. The angles shall be vertically adjustable.

6.3.5 Cage

The cage shall be bolted to the cabinet at 4 points, via the housing cage supports and associated spacer brackets, 2 at the top and 2 at the bottom of the rails.

6.3.6 Cage Position

The cage shall be centered within the cabinet.

CHAPTER 6-SECTION 4
CABINET ASSEMBLIES

6.4.1 General

6.4.1.1 Equipment

The following equipment shall be completely removable from the cabinet without removing any other equipment and using only a slotted or Phillips screwdriver:

Power Supply Assembly
Power Distribution Assembly
Input File
Output File
Monitor Unit Assembly

6.4.1.2 Fuses, Circuit Breakers, Switches and Indicators

All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

6.4.1.3 Equipment in the Cabinet

All equipment in the cabinet, when required shall be clearly and permanently labeled. The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed.

6.4.1.4 Resistor-Capacitor Transient Suppression

Resistor-capacitor transient suppression shall be provided at all AC relay sockets (across relay coil) except for the Flash Transfer Relays (FTR) in the output files where one suppression device may be common for all.

6.4.1.5 Leakage Resistor

A leakage resistor, which permits a small amount of current to pass through the heavy duty relay coil, shall be installed across the terminals of relay sockets to overcome the residual magnetism.

6.4.1.6 Assembly

Assembly or file depth dimension shall include terminal blocks.

6.4.1.7 Air Circulation

All assemblies and files shall allow air circulation through its top and bottom unless specifically called out otherwise.

6.4.1.8 Socket Types

Socket types for the following equipment shall be

Switch Pack	BEAU S-5412-XX (or equal)
Heavy Duty Relay	BEAU S-5408-XX (or equal)
Flasher Unit & Power Sup Mod	BEAU S-5406-XX (or equal)
208 Monitor Unit	PCB 22/44S
210 Monitor Unit	PCB 28/56S

6.4.1.9 Mounting

Connector sockets for Flasher Unit, Power Supply, and Switch Pack modules shall be mounted with their front face 7.5 in deep from assembly or file front panel (Note: Output File Exception).

6.4.1.10 Guides

Guides (Top and Bottom) shall be provided for Switch Pack Modules, Flasher Units, Monitor Unit, Watchdog Timer Module, Detector & Isolator Modules, and Power Supply Module (Bottom only). The guides shall begin 1.0 +/- 0.5 in in from front panel surface and extend to within 0.5 in from the connector socket face.

6.4.1.11 Fabricating

Assemblies and Files shall be fabricated of 0.060 in minimum thickness aluminum or stainless steel sheet. The metal surface shall be treated with clear chromate.

6.4.2 Power Supply Assembly

6.4.2.1 Power Supply

A power supply shall be provided to supply +24 VDC to the Input and Output Files for use by their associated devices. The power supply shall be of ferro-resonant design having no active components and conform to the following requirements:

6.4.2.1.1 Line Load and Design Regulation

Line and Load Regulation – shall not exceed +23.0 to +26.0 VDC (6%) with a design voltage of +24 VDC, specified Load Current range, incoming VAC RMS range and inclusive ripple noise.

6.4.2.1.2 Full Load Current

Full Load Current - 5 Amperes, minimum.

6.4.2.1.3 Ripple Noise

Ripple Noise - 2 volts peak-to-peak and 500 mV RMS at full load.

6.4.2.1.4 Line Voltage

Line Voltage - 90 to 135 VAC.

6.4.2.1.5 Efficiency

Efficiency - 70% minimum.

6.4.2.2 Depth

The assembly shall have a maximum depth of 5.5 in.

6.4.2.3 Front Panel

The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages.

6.4.2.4 Protection

The assembly including terminals shall be protected to prevent accidental contact with energized parts.

6.4.2.5 Power Supply Cage and Transformer

The power supply cage and transformer shall be securely braced to prevent damage in transit.

6.4.3 Power Distribution Assembly (PDA)

6.4.3.1 Equipment

The following equipment shall be provided with the power distribution assemblies:

6.4.3.1.1 PDA #1

1 -- Duplex NEMA 5-15R Controller Receptacle
2 -- Duplex NEMA 5-15R Equipment Receptacle (one with GFI)
1 -- 1 Pole 50 Amperes minimum, 120 VAC Main Circuit Breaker
1 -- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
1 -- 6 Pole Ganged, 15 Amperes, 120 VAC Signal Bus Circuit Breaker
1 -- 2 Pole Ganged, 20 Amperes, 120 VAC Flash Bus Circuit Breaker
1 -- Solid State Relay (Normally Closed) - rated minimum 60 Amperes, 120 VAC
2 -- Model 204 Flasher Unit and Socket
1 -- AUTO/FLASH Control Switch
1 -- FLASH Indicator Light
1 -- Model 430 Heavy Duty Relay (Transfer Relay) & Socket
2 -- 10 Position Terminal Blocks (TBK) T1 & T2

6.4.3.1.2 PDA #2

1 -- Duplex NEMA 5-15R Controller Receptacle
2 -- Duplex NEMA 5-15R Equipment Receptacle (one with GFI)
1 -- 1 Pole 50 Amperes minimum, 120 VAC Main Circuit Breaker
6 -- 1 Pole Ganged, 15 Amperes, 120 VAC Signal Bus Circuit Breaker with Auxiliary Switch
1 -- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
1 -- 2 Pole Ganged, 20 Amperes, 120 VAC Flash Bus Circuit Breaker
1 -- Solid State Relay (Normally Closed) - rated minimum 60 Amperes, 120 VAC
2 -- Model 204 Flasher Unit and Socket
1 -- Model 206 Power Supply Module and Socket
1 -- Model 430 Heavy Duty Relay & Socket (Transfer Relay)
1 -- AUTO/FLASH Control Switch
1 -- Flash On Indicator Light
3 -- 10 Position TBK T1, T2 & T4
1 -- 4 Position TBK T3

6.4.3.1.3 PDA #3

1 -- Duplex NEMA 5-15R Controller Receptacle
2 -- Duplex NEMA 5-15R Equipment Receptacle
1 -- 1 Pole 30 Amperes, 120 VAC Main Circuit Breaker
3 -- 1 Pole 15 Amperes, 120 VAC Circuit Breaker (Equip & Field)
1 -- Model 206 Power Supply Module and Socket
1 -- Model 208 Monitor Unit and Socket
1 -- Model 430 Heavy Duty Relay and Socket (Transfer Relay)
1 -- Watchdog Timer ON/OFF-RESET Control Switch
3 -- Model 200 Switch Pack Sockets
3 -- 10 Position TBK T1, T2 & T4
1 -- 4 Position TBK T3

6.4.3.2 Rating of Breakers

Rating of breakers shall be shown on face of breaker or handle. Breaker function shall be labeled below breakers on front panel.

6.4.3.3 Equipment Receptacle

The first equipment receptacle in the circuit shall have ground-fault circuit interruption as defined in the National Electrical Code. Circuit interruption shall occur on 6 ma of ground-fault current and shall not occur on less than 4 ma of ground-fault current.

6.4.3.4 AUTO/FLASH Switch

The AUTO/FLASH Switch when placed in FLASH position (down) shall energize the Solid State Relay (SSR). When the switch is placed in the AUTO Position (up) the switch packs shall control the signal indications. The switch shall be a SPST Toggle Control Switch.

6.4.3.5 FLASH Indicator Light

The FLASH Indicator Light labeled "Flash On" shall be mounted on the PDA Front Panel. The lamp shall be driven by Flasher Unit/Output through Flash Relay Circuit No. 1 or per Circuit Breaker.

6.4.3.6 Conductors

All conductors from the power distribution assembly routed to the cabinet wiring shall be connected to the terminal block on the common side, except for the AC power conductor between the service terminal block and main circuit breaker. All internal conductors terminating at the blocks shall be connected to the other side of the blocks.

6.4.3.7 Ganged Circuit Breakers

Ganged Circuit Breakers shall be certified by the circuit breaker manufacturer that their circuit breakers shall gang trip.

6.4.3.8 Monitor Unit

The Monitor Unit ON/OFF-RESET Switch shall be a DPST Toggle Control mounted on the PDA #3's front panel. When placed in DOWN Position (OFF-RESET) a grounded input shall be presented at the Monitor Unit Pin 22 (resetting the WDT Circuitry) and the other side switch circuit closes by passing the Monitor Unit.

6.4.3.9 Circuit Breaker with Auxiliary Switch

6.4.3.9.1 Single Pole

Six Single Pole 15 Ampere Circuit Breakers with Auxiliary Switch Feature and Medium Trip Delay Characteristic shall be provided.

6.4.3.9.2 Breakers

The six breakers shall be wired and routed per the Option One Line Diagram. The breaker auxiliary switch circuit shall be open when the breaker is in ON Position. The auxiliary circuits shall be wired in parallel so that any tripped breaker shall energize the Solid State Relay input, Flash Transfer Relay Coils and the "FLASH ON" Indicator. The Auxiliary Contacts shall be rated at 5 Amperes, 120 VAC Minimum (fast on type connection).

6.4.3.9.3 Terminals

Breaker switches shall be bussed using straight solid non-insulated bus wire which is soldered directly to the “fast-on” terminals.

6.4.3.10 Model 206 Power Supply Module

6.4.3.10.1 Requirements

The module shall meet the requirements specified in 6.4.2.1 and 6.4.2.3.

6.4.3.10.2 Module Chassis

The module chassis shall be vented. Its top and sides shall be open except for unit supports

6.4.3.10.3 PDA Assembly

When resident in the PDA assembly, the module shall be held firmly in place by its stud screw, assembly connector support panel and a wing nut.

6.4.3.10.4 Wire-Wound Power Resistors

Two 0.5 Ohm, 10 watt minimum wire-wound power resistors with a 0.2uH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three MOV surge arrestors rated for 20 Joules minimum shall be supplied between AC+ and EG, AC- and EG, and between AC+ and AC-. A 0.68uF capacitor shall be placed across AC+ and AC- between the two power resistors and the MOV's.

6.4.3.11 Terminal Screw Sizes

Terminal screw size shall be 10-32 for TBK T1, T2 & T4 and 6-32 for TBK T3.

6.4.4 Input File

6.4.4.1 Depth

The file shall have a maximum depth of 8.5 in and shall intermit with and support 14 two-channel detector sensor or isolator units.

6.4.4.2 Connectors

The file shall provide a PCB 22/44S connector centered vertically for each two-channel detector. The associated number and letter side connectors shall be shorted internally. Pins D, E, F, J, K, L and W shall be brought out to a 8 position terminal block on the back of the file. The output emitters shall be common grounded with the ground terminating at TB 15, Position 4. Position 8 of the terminal block is assigned to Equipment Ground and is used to terminate lead in shields.

6.4.4.3 Marker Strips

The input file shall be provided with marker strips to identify isolators and detectors in the file.

6.4.4.4 Screw Size

Teminal Block (TB) terminal screw size shall be 8-32.

6.4.5 Output File

6.4.5.1 General Requirements

6.4.5.1.1 Marker Strips

The Output File shall be provided with marker strips to identify switch packs when mounted in the file.

6.4.5.1.2 Connectors

Switch pack connectors, monitor unit connectors, flash transfer relay sockets and flash programming connectors shall be accessible from the back of the Output File without the use of tools or removal of any other equipment.

6.4.5.1.3 Terminal Positions

TBK O1 and O3 terminal positions shall be labeled functionally. A permanent label reading "Channels 9 & 10 Separated" placed on the right Output File mounting flange.

6.4.5.1.4 Field Wire

Field wire terminal blocks shall be mounted vertically on the back of the assembly. Output File #1 shall have 3 terminal blocks with 12 positions and Output File #2 shall have 3 terminal blocks with 6 positions. Terminal position screw size shall be 10-32.

6.4.5.1.5 Flash Transfer Relays

The Flash Transfer Relays shall be Heavy Duty Type. The coil of the relay shall be energized only when the signals are in flashing operation and the police panel ON/OFF switch is ON. The relay shall transfer the field outputs from switch pack output to flash control. The transfer shall not interrupt the controller unit operation.

6.4.5.1.6 Depth

The depth of the file shall not exceed 14.5 in.

6.4.5.1.7 Flash Programming Connectors

The flash programming connectors shall be Molex Type 1375 or equal. The receptacle shall be mounted on the file with a programmable plug connected. The plug connector, with programming jumpers, shall be furnished for each circuit to allow red or yellow flash programming. Plug pins shall be crimped and soldered.

6.4.5.1.8 TB O1,O2,O3& O4 Terminal Screw Sizes

Teminal Block (TB) O1 and O3 terminal screw size shall be 8-32 and TBK O2 & O4 shall be 6-32.

6.4.5.2 Output File #1

6.4.5.2.1 Containing

The output file shall be capable of containing 12 Model 200 Switch Packs, 4 Flash Transfer Relays, and the Model 210 Monitor Unit. Four Flash Transfer Relays and 1 Model 210 Monitor Unit shall be furnished with each output file.

6.4.5.2.2 Output Circuits

The red and yellow output circuits of switch packs 1, 2, 3, 4, 5, 6, 7 and 8 shall be made available at individual pack Molex receptacle /plug connection for flash selectability. Eight red & 4 yellow Molex Plugs shall be provided.

6.4.5.2.3 Model 210 Monitor Unit

It shall be possible to remove the Model 210 Monitor Unit without causing the intersection to go into flashing operation. The cabinet shall be wired so that with the front cabinet door closed and with the monitor unit removed, the intersection shall go into flashing operation (See One Line Diagram). The cabinet shall contain a conspicuous warning against operation with the Model 210 Monitor Unit removed.

6.4.5.2.4 Monitor Unit Compartment

The monitor unit compartment including the housed Model 210 Monitor Unit exclusive of handle shall extend no farther than 1.25 in front of the 19-in rack front surface. The switch pack socket connector front surface shall be no more than 8.5 inches in depth from the front surface of the output file.

6.4.5.3 Output File #2 (Model 420)

6.4.5.3.1 Switch Packs and Flash Transfer Relays

The Output File #2 shall be capable of containing 6 Model 200 Switch Packs and 2 Flash Transfer Relays. Two Flash Transfer Relays shall be provided with the file.

6.4.5.3.2 Output Circuits

The red and yellow output circuits of Switch Packs No. 1, 2, 4 and 5 shall be made available at a Molex receptacle/plug connection for flash select ability.

6.4.6 Heavy Duty Relay (Model 430)

6.4.6.1 Electromechanical Type

Heavy duty relays shall be the electromechanical type designed for continuous duty.

6.4.6.2 Enclosing

Each relay shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating and part number shall be placed on the cover. They shall be permanent, durable and readily visible.

6.4.6.3 DPDT Contacts

Each relay shall be provided with DPDT contacts. Contact points shall be of fine silver, silver alloy or superior alternative material. Contact points and arms shall be capable of switching a 20 Amperes at 120 VAC tungsten load per contact once every 2 seconds with a 50% duty cycle for at least 250,000 operations without contact welding or excessive burning, pitting or cavitation.

6.4.6.4 Relay Coil

The relay coil shall have a power consumption of 10 Volt-Amperes maximum.

6.4.6.5 Potential & Surge Rating

Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or noncarrying parts. Each relay shall have a 1 cycle surge rating of 175 Amperes RMS.

6.4.7 Side Panels

6.4.7.1 Viewing

Two panels shall be provided and mounted on the cage parallel to the cabinet sides. In viewing from the back door, the left side panel shall be designated as the "Input Panel" and the right side panel shall be designated as the "Service Panel".

6.4.8 Cabinet Harnesses

6.4.8.1 C1 Harness

The C1 Harness shall be a minimum of 4 ft in length. The harness wire bundle shall be provided with external protection and routed on the Input Panel Side of the cabinet. Adequate length shall be provided to allow the C1P Connector to properly connect any State Approved Model 170 Controller Unit mounted in the cabinet.

6.4.8.2 Ends

One end of the C1 Harness shall be the C1P Connector with pin contacts wired per the detail assignment. The other ends of the harnesses shall terminate as follows:

Harness #1 - C4S Connector (connected to C4P on Output File #1)
C5S Connector (connected to C5P on either the Input Panel or Output File #2)
Assigned Input Files I & J Positions and Logic Ground Bus

Harness #2 - C5S Connector (same as Harness #1)
C6S Connector (connected to C6P on Output/PDA Assembly)
Assigned Input File I Positions and Logic Ground Bus

Harness #3 - C4S Connector (same as Harness #1)
Assigned Input File I Positions
Input Panel Terminal Block and Logic Ground Bus

6.4.8.3 C1 Harness #3/Output File #2 Adaptor

C1 Harness #3/Output File #2 Adaptor shall be comprised of a C4P Connector on one end and a C5S on the other. The adaptor shall interface the first 24 pins of C4 Connector to the 24 pins of C5.

6.4.8.4 Conductors

Conductors between the C1 Connector and the Input File(s) shall be of adequate length to allow any conductor to be connected to any detector output terminal (Positions S, F, or W).

6.4.9 Monitor Unit Assembly (for Model 336B)

6.4.9.1 Dimensions

The monitor unit assembly shall be 1.75 in high and a maximum of 17.0 in wide. The assembly shall house the Model 210 Monitor Unit (horizontally). A Model 210 Monitor Unit shall be furnished with each assembly.

6.4.9.2 PCB Edge Guides

The assembly shall have a vertical opening of 1.5 in on the front panel for Model 210 insertion/removal. PCB edge guides shall be provided for monitor unit support and to guide it into its mating connector socket.

6.4.9.3 10-Position Terminal Block

A 10-position terminal block (M1) shall be provided on the back plane of the assembly. Position assignment, left to right shall be as follows:

Position 1	-- +24 VDC
Position 2	-- DC Ground
Position 3	-- External Reset
Position 4	-- WDT In
Position 5	-- STOPTIME Output
Position 6	-- Door Switch (Unit Resident)
Position 7	-- Solid State Relay (To PDA)
Position 8	-- AC+
Position 9	-- AC-
Position 10	-- Equipment Ground

6.4.9.4 Circular Plastic Connector

A 37 pin circular plastic connector, matching C4P requirements, shall be provided and mounted rigidly on the back of the assembly. Pin assignments shall be as follows:

PIN	CHANNEL/ FUNCTION	PIN	CHANNEL/ FUNCTION	PIN	CHANNEL/ FUNCTION
1.	1 GREEN	12.	6 YELLOW	23.	12 GREEN
2.	1 YELLOW	13.	7 GREEN	24.	12 YELLOW
3.	2 GREEN	14.	7 YELLOW	25.	13 GREEN
4.	2 YELLOW	15.	8 GREEN	26.	13 YELLOW
5.	3 GREEN	16.	8 YELLOW	27.	14 GREEN
6.	3 YELLOW	17.	9 GREEN	28.	14 YELLOW
7.	4 GREEN	18.	9 YELLOW	29.	15 GREEN
8.	4 YELLOW	19.	10 GREEN	30.	15 YELLOW
9.	5 GREEN	20.	10 YELLOW	31.	16 GREEN
10.	5 YELLOW	21.	11 GREEN	32.	16 YELLOW
11.	6 GREEN	22.	11 YELLOW	33.	AC-

NOTE: PINS 34 TO 37 NOT ASSIGNED

CHAPTER 6-SECTION 5
CABINET WIRING

6.5.1 Cabinet Wiring Diagram

6.5.1.1 Diagrams/Drawings Supply

Four sets of nonfading (comparable to Xerox 2080) cabinet wiring diagram and drawing sheets shall be supplied with each cabinet. The diagrams shall be nonproprietary. They shall identify all circuits in such a manner as to be readily interpreted. The cabinet drawing sheets shall show the equipment layout in an elevation view as viewed from the rear of the cabinet with the left and right cabinet walls shown in their relative positions.

The diagram and drawing sheets shall be placed in a heavy duty side opening clear plastic pouch and attached to the front cabinet door.

6.5.1.2 Pouch

A pouch that would hold the Cabinet Manuals, Cabinet Wiring and Drawing Sheets, and Cabinet Keys shall be provided as part of the Cabinet.

The pouch shall be of such design and material that it provides adequate storage and access to the wiring diagram sheets and cabinet manuals. The pouch shall be of size and strength to easily hold the documents and keys without tearing.

6.5.1.3 Manuals

Two cabinet manuals shall be provided in the pouch together with the wiring diagram and drawing sheets.

6.5.2 Conductors

6.5.2.1 General

All conductors used in cabinet wiring shall terminate with properly sized non-insulated (if used, for DC Logic Only) or clear insulated spring-spade type terminals except when soldered to a through-panel solder lug on the rear side of the terminal block or as specified otherwise. All crimp-style connectors shall be applied with a power tool which prevents opening of the handles until the crimp is completed.

6.5.2.2 Sizes

Conductors between the service terminal AC- and Equipment Ground and their associated bus, the equipment ground bus conductor to Power Distribution Assembly and cage rail, AC- Bus to Power Distribution Assembly shall be No. 8 or larger.

6.5.2.3 Types

All conductors unless otherwise specified shall be No. 22, or larger, with a minimum of 19 copper strands. Conductors shall conform to Military Specification: MIL-W-16878D, Type B, or better. The insulation shall have a minimum thickness of 10 mils and shall be nylon jacketed polyvinyl chloride except that Conductors No. 14 and larger may have Type THHN insulation (without Nylon Jacket), and shall be stranded with a minimum of 7 copper strands.

6.5.2.4 Labels

All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

6.5.2.5 Color-Code Requirements

All conductors shall conform to the following color-code requirements:

6.5.2.5.1 Grounded Conductors

The grounded conductors of AC circuits shall be identified by a solid white or solid gray color.

6.5.2.5.2 Equipment Grounding

The equipment grounding conductors shall be identified by a solid green color or by a continuous green color with 1 or more yellow stripes.

6.5.2.5.3 DC Logic Ground

The DC logic ground conductors shall be identified by a solid white color or continuous white color with a red stripe.

6.5.2.5.4 Ungrounded AC+ Conductors

The ungrounded AC+ conductors shall be identified by a solid black or continuous black with colored stripe.

6.5.2.5.5 Logic Ungrounded Conductors

The logic ungrounded conductors shall be identified by any color not specified above.

6.5.2.6 DC Logic Ground and Equipment Ground

Within the cabinet, the DC logic ground and equipment ground shall be electrically isolated from the AC grounded conductor and each other by 500 MegaOhms when tested at 250 VDC.

6.5.2.7 AC- Copper Terminal Bus

The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 0.25 in shall be used for securing the bus to the service panel.

6.5.2.8 Power Supply DC Ground

The cabinet power supply DC Ground shall be connected to the DC logic ground bus using a No. 14, or larger, stranded copper wire.

6.5.2.9 Input Terminal

Each detector lead-in pair, from the field terminals in the cabinet to the sensor unit rack connector, shall be a cable of UL Type 2092 or better. The stranded tinned copper drain wire shall be connected to a terminal on the input file terminal block. This input terminal shall be connected to the equipment grounding bus through a single conductor.

6.5.3 Terminal Blocks

6.5.3.1 Terminal Screws

The terminal blocks shall be barrier type rated at 20 Amperes, 600 volts RMS minimum. The terminal screws shall be 0.3125 in minimum length nickel plated brass binder head type with screw inserts of same material. Screw size is called out under associated cabinet assembly, file or side panel.

CHAPTER 6-SECTION 6
SERVICE PANEL ASSEMBLY

6.6.1 General Requirements

A Service Panel Assembly shall be provided. The assembly shall function as the entry point for AC Power to the cabinet including main and secondary circuit breakers, cabinet transient and voltage surge protection, clean power filtering, and Raw and Clean AC Power Sources.

6.6.2 Location

The assembly shall be located on the lower right Cage when viewed from the back door.

6.6.3 Service Terminal Block

The terminals of the Block shall be labeled AC+, AC-, and EQ GND and shall be covered with a clear insulating material to prevent inadvertent contact. The Terminating Lugs shall be large enough to accommodate # 2 conductors.

6.6.4 Surge Protector

One type of surge protector shall be the EDCO Model SHA-1250 or equal allowed.

6.6.4.1 Impulse Breakdown

Less than 1,000 volts in less than 0.1 us at 10 kilovolts/us.

6.6.4.2 Standby Current

Less than 1 mA.

6.6.4.3 Striking Voltage

Greater than 212 VDC.

6.6.4.4 Ranges

Capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes.

CHAPTER 6-SECTION 7
332, 334, & 336 CABINET DETAILS

CHAPTER 7
REFER TO ITS CABINET STANDARD

CHAPTER 8
REFER TO CHANGEABLE MESSAGE SPECIFICATIONS

CHAPTER 9
MODEL 2070 CONTROLLER
SPECIFICATIONS

CHAPTER 9-SECTION 1
GENERAL

9.1.1 Controller Unit

The Controller Unit shall be composed of the Unit Chassis, modules and assemblies per their version. The following is a list of 2070 Versions, their interface rolls and composition:

UNIT VERSION	DESCRIPTION
2070V UNIT	Provides directly driven VME and mates to 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1A TB, 2070-1A MCB, 2070-2A FI/O, 2070-3A FRONT PANEL, 2070-4 POWER SUPPLY, and 2070-5 VME CAGE ASSEMBLY.
2070L UNIT	LITE Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY
2070LC UNIT	LITE unit mates to ITS cabinets only. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2B FI/O, 2070-3C FRONT PANEL and 2070-4 POWER SUPPLY
2070LX UNIT	LX Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1C CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY
Note: See Chapter 11 for 2070 NEMA Versions	

9.1.2 Communications and Option Modules

The communications and option modules shall be called out separately from the unit version. The composition weight shall not exceed 25 lbs.

9.1.3 Chassis

The Chassis top and Bottom, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel shall be made of 0.060 inches minimum aluminum sheet. The Chassis Side panels shall be 0.090 inches minimum sheet

9.1.4 Power Failure Power Restoration Operations

It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules shall comply to said operations.

9.1.5 2070 Unit Module

2070 UNIT module / assembly power limitations shall be as follows:

Models	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
2070-1A MCB	750 mA	-----	-----	-----
2070-1A TB	750 mA	-----	-----	-----
2070-1E CPU	1.0 A	250 mA		
2070-1C, Host Board	2A	250mA		
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A,B&D FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	500 mA	-----	50 mA	50 mA
2070-5 VME Cage	5.0 A	-----	200 mA	200 mA
2070-6A & Others	1A	-----	200 mA	200 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA
Model 2070 -6 & Others shall not exceed 6 Watts Max usage.				

9.1.6 EIA-485 Communications Links

All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 Mbps. Isolation circuitry shall be by opto- isolation technologies.

9.1.7 EIA-485 Line Drivers/Receivers

The EIA-485 Line Drivers/Receivers shall be socket mounted or Surface mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

9.1.8 Sockets

Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9.1.9 Frame Address

SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

	SP 5	SP3
CPU 2070-1	“19"	“19”
FI/O 2070-2A	"20"	“NA”
Manufacturer Use	128 -254	128-254
CPU Broadcast to all	"255"	“255”

All other addresses are reserved or assigned by the Agency with the exception of NEMA TS2 Type 1 Requirements (See Chapter 11). The SDLC response shall contain the frame address of the Command sender.

CHAPTER 9-SECTION 2
MODEL 2070-1 CPU MODULE

9.2.1 Model 2070-1A CPU Module

The Model 2070-1A CPU Module shall consist of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

9.2.1.1 Main Controller Board (MCB)

The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master& Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester and BTO **(**64)

9.2.1.2 Controller

The Controller Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for State use only. The Interrupts shall be configured as follows:

Level 7 - VMEbus IRQ7	
Level 6 - VMEbus IRQ6	ACFAIL
Level 5 - VMEbus IRQ5	CPU: Module Counters Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4 - VMEbus IRQ4	
Level 3 - VMEbus IRQ3	
Level 2 - VMEbus IRQ2	
Level 1 - VMEbus IRQ1	

9.2.1.3 Memory Address Organization

8000 0000	80FF FFFF	STANDARD
9000 0000	9000 FFFF	SHORT

9.2.1.4 Transition Board

A Transition Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Motherboard. Said signal and communication lines shall be driven/received off and on the module compliant to EIA-485. The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 &A3 Installed lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

9.2.1.5 Shielded Interface Harness

A Shielded Interface Harness shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm (0.984 in) of slack shall be provided. No power shall be routed through the harness. The harness shall be 100% covered by an aluminum Mylar foil and an extruded black 0.8 mm (0.0315 in) PVC jacket or equal.

9.2.2 Model 2070-1E CPU Module

The Model 2070-1E CPU Module shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the Motherboard Slot A5. The module shall meet all the requirements listed under this section and Chapter Details Section 7. The Model 2070-1E Module shall have a Motorola MC68EN360 CPU or equal, clocked at 24.576 MHz minimum.

9.2.2.1 Dual SCC Device

A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1 except where noted. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68EN360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements except where noted, including EIA 485 drivers / receivers and synchronous data rate of 614.4 Kbps. An internal DIP Switch shall be provided to disconnect SP8 RTS, CTS and DCD (Pins 5, 6, 7, 18, 19 and 20) lines from C13S Connector. The DIP Switch shall not require a poking device to be switch ON/OFF.

9.2.2.2 68EN360 SCC1

The 68EN360 SCC1 shall be reassigned to Ethernet (ENET) Network meeting Ethernet 10 Mbps IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software. The CPU network lines shall be connected to a port on the Network Switch. Four LEDs labeled “10/100 and Link/Act” shall be mounted on the front panel signifying Ethernet operational conditions between the CPU and the Network Switch.

9.2.2.3 Module 2070 -1E Power Requirements.

The 2070-1E CPU Module shall not draw more than 1.00 A of +5VDC & 250 mA of ISO+12 VDC.

9.2.2.4 The C13S Connector

The C13S Connector shall be a DB25S connector and shall be located on the Module 2070 -1X CPU front panel and shall contain signals for SP8, LINESYNC, NRESET, POWERDOWN, and an isolated BIAS +5VDC as specified in the following subsections and as listed in A9-7.

9.2.2.4.1 Serial Port SP8

System Serial Port 8 (SP8) shall be isolated, converted to EIA-485, and then routed to Connector C13S. SP8 shall meet all SP2 Port requirements except where noted.

9.2.2.4.2 LINESYNC and POWERDOWN

LINESYNC and POWERDOWN lines shall each be isolated, converted to EIA-485, and then routed to connector C13S for external module use.

9.2.2.4.3 NRESET

CPU_Reset and POWER UP lines shall be isolated, then OR’d to form NRESET. NRESET shall then be converted to EIA-485 and routed to connector C13S for external module use.

9.2.3 Model 2070-1C CPU Module

The TYPE 2070-1C CPU Module shall be a single board module meeting the 2X WIDE board requirements. The module shall be furnished normally resident in MOTHERBOARD Slot A5. The module shall meet the requirements as listed Section 9.2.2.4 of these specifications.

9.2.3.1 Engine Board

The TYPE 2070-1C CPU shall use an Engine Board compliant to the AASHTO/ITE/NEMA Next Generation ATC Standard with the exceptions as defined in Sections 9.2.5 and 9.2.8. The Engine Board shall be used for execution of the application software. No other microprocessor or memory of the 2070-1C CPU shall be used for execution of the application software.

9.2.3.2 Ethernet Ports

The ETHERNET ports of the Engine Board shall be brought out on an RJ 45 Connectors mounted on the 2070-1C front panel. The front panel LED indicators for the two Ethernet ports shall conform to the AASHTO/ITE Next Generation ATC Standard.

9.2.3.3 Universal Serial Bus (USB)

The TYPE 2070-1C CPU Module shall include a USB port compliant to the AASHTO/ITE Next Generation ATC Standard with the exceptions that USB shall conform to the appropriate sections of the USB v2.0 specification for both hardware and software operations. USB shall be brought out from the Engine Board to a USB Connector mounted on the 2070-1C front panel.

9.2.3.4 Host Module

The 2070-1C CPU Module shall use a Host Module that provides the mechanical and electrical interfaces to the Engine Board and Motherboard. The Host Module shall convert the 5VDC as provided by the Model 2070-4A power supply to 3.3VDC as required by the Model 2070-1C Engine Board and all of its components.

The TYPE 2070-1C CPU Module shall implement the host module identification using the Engine Board SPI serial port, compliant to the AASHTO/ITE Next Generation ATC Standard.

9.2.4 Model 2070-1A and 2070-1E CPU Module

9.2.4.1 Contiguous Addresses

16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's Supplied File Manager.

9.2.4.2 Incoming +5 VDC

When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. A on-board circuit shall sense the +5 VDC Standby Power and shift to a On-board CPU Power Source. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

9.2.4.3 Ram Memory

A minimum of 8 MB of DRAM memory, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM will be available for agency use, organized in 16 or 32-bit words shall be provided. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

9.2.4.4 Flash Memory

A minimum of 8 MB of FLASH memory, organized in 16- or 32- bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 2 MB of FLASH Memory shall be used for the Boot Image and a minimum of 6 MB shall be available for Agency use. A maximum of 2 MB of Flash Memory shall be reserved the Boot Image only. Flash memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better."

9.2.4.5 Time-of-day Clock

A software settable hardware Time-of-Day (TOD) clock shall be provided. It shall, under on-board standby power maintain an accuracy of ±1 minute per 30 days at 25°C. The clock shall provide a minimum fractional second resolution of 10 ms and shall track seconds, minutes, and hours, day of month, month, and year.

9.2.4.6 CPU_Reset

A software-driven CPU_Reset signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be a driver capable of sinking 30 mA at 30 VDC. Execution of the program module "cpureset" in the boot image shall assert the CPU_Reset signal once. CPU_Reset shall be executed when the controller starts up or is rebooted using the OS-9 break command.

9.2.4.7 CPU_ACTIVE LED Indicator

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED Indicator. The LED shall default to ON when the controller starts up.

9.2.4.8 Tick Timer

The OS-9 Operating System Tick Timer interrupt shall be derived from the each transition of LINESYNC signal, with a tick rate of 120 ticks per second.

9.2.4.9 SRAM and TOD Clock

The SRAM and TOD Clock Circuitry under Standby mode shall draw no more than 8uA at 2.5 VDC and 35 degrees C. An On board Capacitor supply shall hold up SRAM and TOD for a minimum of 7 days.

9.2.4.10 Network Switch, Model 2070 -1E

The Model 2070-1E CPU Module shall be provided with an integrated Store-and-Forward Network Switch per the IEEE 802.3, 802.3u and 802.3 x specifications.

The switch shall be configured with two ports connected to the front panel RJ-45 connectors (C14S) and a third port shall be connected to the CPU. A forth Port on the Network Switch shall be used to route Ethernet across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively.

9.2.5 Model 2070-1C CPU Module

9.2.5.1 Model 2070-1C CPU Module Processor

The Model 2070-1C CPU Module Processor shall consist of a Freescale series MPC 82xx / 83xx with a minimum MIPS of 400 calculated using the Dhrystone v2.1 benchmark at 25°C.

9.2.5.2 Ram Memory (DRAM)

The Model 2070-1C CPU Module shall contain a minimum of 64Mbytes of DRAM or equivalent volatile memory for application and OS program execution.

9.2.5.3 Flash Memory

The Model 2070-1C CPU Module shall contain a minimum of 32Mbytes of FLASH for storage of OS Software and user application.

9.2.5.4 Static Memory (SRAM)

The Model 2070-1C CPU Module shall contain a minimum of 1Mbytes minimum of SRAM memory for non-volatile parameter storage.

9.2.5.5 Standby Power

The Model 2070-1C CPU Module Engine Board shall provide the Standby Power required for supporting the SRAM and RTC.

9.2.5.6 Network Switches, Model 2070-1C

The Model 2070-1C CPU Module shall be provided with two integrated 3 port Store-and-Forward Network Switches per the IEEE 802.3, 802.3u and 802.3 x specifications. One switch shall be configured with port 1 and 2 connected to the front panel RJ-45 connectors and port 3 shall be connected to the CPU ENET 1 port. The second switch shall be configured with port 1 connected to the front panel RJ-45, port 2 shall be connected to the CPU ENET 2 port. Port 3 shall be used to route Ethernet across the Motherboard to the “A” Connectors. DC Grounding plane around the network connectors and lines shall be provided. Port 3 Network Lines shall be assigned to: NetP5 TX+, TX-, RX+ and RX- respectively.

9.2.5.7 Real-Time Clock (RTC)

The Model 2070 -1C Module shall be provided with a software settable, hardware RTC that meets the requirements of the ASHTO/ITE/NEMA ATC Standard except that in the absence of VPRIMARY, the RTC shall operate from VSTANDBY as listed in A9-16 of these specifications. Also Operating System Time shall be maintained by utilizing the RTC and LINESYNC as defined in Section 9.5.5.3.

9.2.5.8 CPU_Reset

A software-driven CPU_Reset Signal (Active Low) shall be provided to reset other system devices and shall be accessible by application programs as well as by the command line as “cpureset”. CPU_Reset shall be executed when the Controller starts up or is rebooted using the reboot command.

9.2.5.9 CPU_ACTIVE

An Active Low signal shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED indicator. This signal shall cause to the LED to default to ON when the controller starts up.

9.2.5.10 Application Program Interface (API)

The Model 2070-1C Module shall be fully compliant and shall be provided, upon request, with an installed copy of the Application Program Interface (API) compliant to the latest ASHTO/ITE ATC API Standard.

9.2.5.11 Integrated Security

The Model 2070-1C Module shall be implemented with integrated security support for DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms as well as a public key accelerator and an on-chip random number generator.

9.2.5.12 SD Card Support

The Model 2070-1C Module shall support SD Card Memory and shall be provided with an industry standard SD Card socket.

9.2.6 Data Key

A Datakey Keyceptacle™ (KC4210, KC4210PCB or equal) shall be mounted on the CPU module front panel (or the Transition Board of MODEL 1A). Power shall not be applied to the receptacle if the key is not present.

The contractor shall supply a 8Mb Memory Size Datakey (SFK8Mb or equal) with each MODEL 1A TB (Transition Board) or 1E and 1C CPU module unless specified otherwise. The Datakey shall be temperature rated for –40 °C to +85 °C (–40°F to 185 °F) operation, shall be blue in color, and shall be initialized to the format and default values defined below. External capability to program the CPU Datakey shall be provided by the contractor.

When programmed, the memory on the key of header shall be organized as follows:

Bytes	Description	Default Values
1-2	16 bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64	
3	Key Type	See table below
4	Header Version	2
5-8	Latitude	0.0
9-12	Longitude	0.0
13-14	Controller ID	0xFFFF
15-16	Communication drop number	0xFFFF
17-20	IP Address	10.20.70.51
21-24	Subnet Mask	255.255.255.0
25-28	Default Gateway	10.20.70.254
29	Startup Override	0xFF
30-64	Reserved for Agency use	All bytes set to 0xFF
65 to End	User Data	All bytes set to 0xFF

When programmed, Byte 3 of the header shall contain the Key Type value as defined in the following table:

Key Type	Model No.	Memory Size	Sector Size	Part Number
1.	DK1000	1Kb	2 Byte	611-0006-002A
2.	LCK16000	16Kb	2 Byte	611-0070-008A
3.	SFK2Mb	2Mb	64KBytes	611-0089-004A
4.	SFK4Mb	4Mb	64KBytes	611-0104-002A
5.	SFK8Mb	8Mb	64KBytes	611-0132-006A
6.	SFK32Mb	32Mb	64KBytes	611-0164-005A

The data format in the CPU Datakey header for the Latitude and Longitude fields shall comply with IEEE/ANSI 754-1985 STD. All the other fields shall follow a Big Endian Format as implemented by Motorola CPUs.
The Startup Override byte, not the Key Type, may be used to override the default controller startup procedure, as described in section 9.2.7.3.3.

9.2.7 Model –1A and 2070-1E CPU Module Software

The following shall be supplied:

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Deliverables
5. Error Handler

9.2.7.1 Operating System

The CPU Module shall be supplied with Microware Embedded OS-9 Release 1.3 or later with kernel edition #376 or later. The following modules shall be included:

1 Embedded OS-9 Real Time Kernel
2 Sequential Character File Manager (SCF)
3 Stacked Protocol File Manager (SPF)
4 Pipe File Manager (PIPEMAN)
5 Random Block File Manager (RBF)
6 C Shared Library (CSL)

Boot Image shall include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Format	Dcheck	Login	Link	Kermit
Tsmon	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime	Merge	Grep	
Tee	Printenv				

The Boot Image with the above utilities and including the network driver and descriptor shall be loaded into RAM as part of OS-9 initialization as defined in Section 9.2.7.3.2.

9.2.7.2 Drivers and Descriptors

9.2.7.2.1 Supplied Modules

Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.
Device drivers which require extensions to the standard Microware libraries shall use the _os_getstat() and _os_setstat() functions.
A custom setstat code and parameter structure are defined as follows:

```
#define SS_2070     0x2070

error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);

error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

typedef struct
{
    u_int32 code;
    u_int32 param1;

    union
    {
        u_int32 param;
        void  *pointer;

    } param2;
} PB2070, *pb;
```

The following subcodes for use with PB2070.code are also defined:

```
#define GS2070_Status          0x1C
#define SS2070_SSig            0x1A
#define SS2070_IFC             0x22
#define SS2070_OFC             0x23
#define SS2070_Timer_Null      0x0000    (Default State)
#define SS2070_Timer_Sig       0x1000
#define SS2070_Timer_Cyc       0x1001
#define SS2070_Timer_Start     0x1002
#define SS2070_Timer_Stop      0x1003
#define SS2070_Timer_Reset     0x1004
```

Note: When PB2070.param2.pointer is used, PB2070.param1 should be loaded with the size of what PB2070.param2.pointer is referencing. When calling _os_getstat() or _os_setstat(), all reserved or unused parameters and fields in PB2070 should be loaded with 0 (zero).

9.2.7.2.2 Memory Drivers

Drivers shall be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors shall apply:

/f0	FLASH drive	non-volatile, writeable
/dd	FLASH drive	OS-9 default device for /f0
/f0wp	FLASH Drive	as /f0 except write protected
/f0fmt	FLASH Drive	as /f0 except format enabled
/r0	SRAM Drive	non-volatile ramdisk
/r0fmt	SRAM Drive	as /r0 except format enabled
/r2	DRAM Drive	volatile 2 MB ramdisk, not automatically initialized

9.2.7.2.3 MC68360 Internal Timers

A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Timer resolution shall be one count equals 100 µS and all timer periods shall be specified in units of hundreds of microseconds (µS), i.e. a timer period of 7 = 700µS. The minimum allowed timer period shall be 500µS. The Maximum Timer Period for timers 1-4 shall be 6.5535 seconds (0xFFFF). The Maximum Timer Period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF). The driver shall return error E$Param from os_setstat() if the requested timer period is outside the allowable range.

A signal of "0" shall be an invalid signal and the driver shall return an E$PARAM error if received.

Access to the MC68360 internal timers shall be through the following descriptors:

The timers should be set to SS2070_Timer_Null Mode upon initialization.

9.2.7.2.3.1 Descriptor

Descriptor names for each timer:

timer1	= access to MC68360's internal timer #1
timer2	= access to MC68360's internal timer #2
timer3	= access to MC68360's internal timer #3
timer4	= access to MC68360's internal timer #4
timer12	= access to MC68360's internal timer #1 & #2 [cascaded]
timer34	= access to MC68360's internal timer #3 & #4 [cascaded]

9.2.7.2.3.2 Timer Standard

Timer Standard OS-9 Function Calls:

error_code _os_open (char *timer_desc_name, path_id *path);

error_code _os_read (path_id path, void *timer_value, u_int32 *size);

Note: Prior to calling _os_read(), size must be loaded with the value 4 and timer value must be pointed to a u_int32. _os_read() shall read the current timer value and load it into timer_value as µS x 100.

error_code _os_close (path_id path);

9.2.7.2.3.3 Time Extension

Timer Extension to Standard OS-9 Function Calls:

The timer drivers shall support the following modes using the following function with the SS_2070 option code and a custom parameter block structure:

error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

a. Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal. After one-shot signal is sent, timer shall stop (SS2070_Timer_Stop).

```
pb→    code = SS2070_Timer_Sig;          /* request for one-shot signal */
pb→    param1= signal;
pb→    param2.param = period;
```

b. Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal.

```
pb→    code = SS2070_Timer_Cyc (0x1001);    /* request for periodic signal */
pb→    param1 = signal;
pb→    param2.param = period;
```

c. Start timer. Starts the timer if stopped or null. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period. Timer will not send a signal and any pending signals will be cancelled.

```
pb→ code = SS2070_Timer_Start;          /* start timer if stopped */
```

d. Stop timer. Leaves current value in timer. Cancels any pending signals.

```
pb→ code = SS2070_Timer_Stop;           /* stop timer if running */
```

e. Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals.

```
pb→ code = SS2070_Timer_Reset           /* reset timer (stop and zero) */
```

9.2.7.2.3.4 Timer Extension

Timer Extension to Standard OS-9 Function Calls:

The timer driver shall support the following function with the SS_2070 option code and custom parameter block structure:

```
error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);
```

a. Retrieve current timer configuration.

```
typedef struct
{
        u_int32 value;
        u_int32 mode;
        u_int32 signal;
        u_int32 period;
} Timer_status;

pb→ code = GS2070_Status  (0x1C)     /* Request timer status data */
pb→ param1 = sizeof(Timer_status)
pb→ param2.pointer = &Timer_status *
```

Status data shall be returned in the structure pointed to by pb→param2.pointer as follows:

```
pb→ param2.pointer→value     /* current timer value in µS x 100 */
pb→ param2.pointer→mode      /* SS2070_Timer_Sig if one-shot signal pending,
                             SS2070_Timer_Cyc if periodic signal pending,
                             SS2070_Timer_Start if free running,
                             SS2070_Timer_Stop if not active
                             SS2070_Timer_Reset if timer is reset
                             SS2070_Timer_Null when timer is first
                             initialized */

pb→ param2.pointer→signal    /* signal code pending if
```

		SS2070_Timer_Sig or SS2070_Timer_Cyc, 0 otherwise */
pb→	param2.pointer→period	/* timer period in µS x 100 if SS2070_Timer_Sig or SS2070_Timer_Cyc and Maximum Timer Period if SS2070_Timer_Start , 0 otherwise */

The following values shall be returned when the timer is in the SS2070_Timer_Null (Timer initialized) Mode:

Timer Mode =	SS2070_Timer_Null
Timer Value =	0
Timer Period =	0
Timer Signal =	0

The following values shall be returned when the timer is in the SS2070_Timer_Start Mode:

Timer Mode =	SS2070_Timer_Start
Timer Value =	Running Timer Value
Timer Period =	Maximum Timer Period
Timer Signal =	0

The following values shall be returned when the timer is in the SS2070_Timer_Stop Mode:

Timer Mode =	SS2070_Timer_Stop
Timer Value =	Current Timer Value
Timer Period =	0
Timer Signal =	0

The following values shall be returned when the timer is in the SS2070_Timer_Reset Mode:

Timer Mode =	SS2070_Timer_Reset
Timer Value =	0
Timer Period =	0
Timer Signal =	0

9.2.7.2.3.5 Timer Period

All timer periods are specified in units of hundreds of microseconds (µS), i.e. a timer period of 7 = 700µS. The minimum allowed timer period shall be 500µS. The maximum timer period for timers 1-4 shall be 6.5535 seconds (0xFFFF). The maximum timer period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF). The driver shall return error E$Param from _os_setstat() if the requested timer period is outside the allowable range.

9.2.7.2.4 CPU Datakey

Access and control to the CPU Datakey shall be provided through the following descriptor name and OS-9 functions:
Descriptor name:
datakey = access to the CPU Datakey

Function Calls:

error_code = _os_open (char *datakey_desc_name, path_id *path);

error_code = _os_close (path_id path);

error_code = _os_read (path_id path, void *data_buffer, u_int32 *data_size);

error_code = _os_write (path_id path, void *control, u_int32 *data_size);

error_code = _os_seek(path_id path, u_int32 *position); sets read / write offset

error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); erases sector(s) if pointer is on a block boundary, returns E$PARAM error if not on a boundary */

error_code = _os_gs_pos(path_id path, u_int32 *position); /* gets current file pointer position */

error_code = _os_gs_size(path_id path, u_int32 *size); /* gets current datakey size */

Error codes returned by Function calls:

E$NotRdy if datakey is not inserted
E$Seek if Offset plus *data_size is beyond end of CPU Datakey.
E$EOF if upon read or write, the last byte of CPU Datakey has previously been processed.
Note: Use of SCF to implement the datakey driver is not allowed.

9.2.7.2.5 Flow Control Modes

The asynchronous serial communications device drivers shall support the six flow control modes (FCM#) described below:

FCM#	Description
1.	No Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed. This is the default mode. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode (FCM# 1).
2.	Manual Flow Control Mode: The driver transmits data regardless of the state of CTS. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
3.	Auto-CTS Flow Control Mode: The driver transmits data only when CTS is externally asserted. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
4.	Auto-RTS Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If the user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
5.	Fully Automatic Flow Control Mode: The driver transmits data only when CTS is externally asserted. Upon a write command, the driver asserts RTS and waits for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
6.	Dynamic Flow Control Mode: The driver transmits data only when CTS is externally asserted. The driver controls RTS based on the status of its receiving buffer. The driver asserts RTS continuously as long as its receiving buffer has sufficient capacity to store incoming data. If the receiving buffer approaches full, the driver de-asserts RTS until enough data has been read from the buffer to create sufficient receive capacity.

9.2.7.2.5.1 Serial Device Driver

The serial device driver shall be able to set user options via _os_setstat() and return status via _os_getstat(). To support legacy application programs, the device driver shall also be able to set user options via _os_ss_size() and to return status via _os_gs_size():

```
error_code_os_setstat(path_id path, SS_2070, void *pb);
error_code_os_getstat(path_id path, SS_2070, void *pb);
error_code_os_ss_size(path_id path, u_int32 size);
error_code_os_gs_size(path_id path, u_int32 *size);
```

Note: The preferred method of accessing serial device drivers is through _os_setstat() and _os_getstat(). The _os_ss_size() and _os_gs_size() interface may not be required by future versions of this specification and is therefore not recommended for new development.

The option subcodes to be passed in pb→code and the data to be contained in pb→param1 are defined as follows. pb→param2 is unused here and should be set to 0 (zero). For _os_ss_size() and _os_gs_size(), the size argument is the same format as pb→param1.

9.2.7.2.5.2 Supported Setstat

The supported _os_setstat() / _os_ss_size() options shall be as follows.

a. **Subcode passed in pb→code is SS2070_OFC (0x23).**

1. If CTS is currently negated and bits 16-31 are not all 0:
Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.
Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.

2. If CTS is currently asserted and bits 16-31 are not all 0:
Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal immediately.
Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot as soon as CTS is negated.

3. If both bits 11 and 12 of the SS2070_SSig parameter block are set, and bits 16-31 are not all 0:
The controller will send a one-shot signal upon the next change of CTS state

Data passed in pb→param1 is defined as follows:

Bits	Description
31-24	Auto RTS turn-off extension in number of characters (range:0-255, 0=default).
23-14	Reserved for future use.
13	Inhibit return of error E$Write from _os_write() when transmit buffer full in FCM# 2, 4, 5 (default=0, 0=error, 1=block)
12	Inhibit variable SCC MRBLR (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range:0-5).
7-0	Subcode SS2070_OFC (0x23).

9.2.7.2.5.3 Variable MRBLR (68360 SCC)

To reduce the IRQ handler overhead, the 68360 SCC driver shall use variable MRBLR as follows. If SS2070_OFC bit 12 is set to 1, the MRBLR shall be fixed at 16 for all baud rates. Variable MRBLR is not required for SP1 or SP8 on the 2070-1B CPU Module.

Baud Rate	MRBLR Setting
1200	1
2400	2
4800	4
9600	8
19200 & Higher	16

9.2.7.2.5.4 TODR (68360 SCC only):

TODR requests processing a new TX buffer immediately. To reduce impact on other serial channel operations, SS2070_OFC bit 11 may be set to 1 to prevent assertion of TODR. TODR is not required for SP1 or SP8 on the 2070-1B CPU Module.

b. Subcode passed in pb→code is SS2070_IFC (0x22).
Data passed in pb→param1 is defined as follows:

Bits	Description
31-11	Reserved for Future Use.
10	DCD must be asserted to receive data (default=0; 0=NO; 1=YES).
9-8	Reserved for Future Use.
7-0	Subcode = SS2070_IFC (0x22).

c. **Subcode passed in pb→code is SS2070_SSig (0x1A).**
Data passed in pb→param1 is defined as follows:

Bits	Description
31-16	A signal number to be sent to calling process when the state of an input changes.
15-13	Reserved for Future Use.
12	Send signal when CTS is de-asserted.
11	Send signal when CTS is asserted.
10-8	Reserved for Future Use.
7-0	Subcode = SS2070_SSig (0x1A).

9.2.7.2.5.5 Supported Getstat

The supported _os_getstat()_ / _os_gs_size() options shall be as follows.

a. **Subcode passed in pb→code is GS2070_Status (0x1C).**
Data returned in pb→param1 is defined as follows:

Bits	Description
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use.
10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Use.
6	Overrun error –0=no error; 1=error has occur since last GS2070_Status call.
5	Frame error –0=no error; 1=error has occur since last GS2070_Status call.
4	Parity error –0=no error; 1=error has occur since last GS2070_Status call.
3-2	Reserved for Future Use.
1	DCD state –0=de-asserted; 1=asserted.
0	CTS state –0=de-asserted; 1=asserted.

9.2.7.2.6 Device Drivers Compliant

Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator

dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

error_code _os_open (char *desc_name, path_id *path); //open descriptor for command

error_code _os_close (path_id path); //close descriptor

error_code _os_write (path_id path, void *value, u_int32 *data_size); //set value of function

*value = 1, turn on LED or enable DST correction (default)

*value = 0, turn off LED or disable DST correction set u_int32*data_size to 1

error_code _os_read (path_id path, void *value, u_int32 *data_size); //get current state set u_int32*data_size to 1

9.2.7.2.7 Manufacturer Support

The manufacturer shall provide the following features to support the TOD operation and synchronization.

9.2.7.2.7.1 Leap Year and Daylight Savings Time

Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years.

9.2.7.2.7.2 Setting Hardware Clock

Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be “ClockUpdate.” Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

9.2.7.2.7.3 Setting OS-9 System Clock

Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall be synchronized to a minimum of 10 ms resolution.

9.2.7.2.8 Flash Ram Drive

The FLASH drive shall be protected from corruption. It shall be protected using the Write Protect (WP) bit of the Base Register. When writing to the FLASH drive the current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy.

A user write operation shall restore the valid backup sector copy first. Execution of the program module, “FLRESTORE,” in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. “FLRESTORE” shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds.

9.2.7.3 OS-9 Application Kernel

9.2.7.3.1 Boot Sysreset

The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the following defaults:

SP 1 & 2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP 3S	614.4 Kbps
SP 4	9.6 Kbps, 8-bit word, 1 stop, no parity, no pause, x on and x off BOTH OFF
SP 5S	614.4 Kbps
SP 6	38.4 Kbps, 8-bit word, 1 stop and no parity

9.2.7.3.2 Hardware Initialization

Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 4 seconds. This startup time shall be measured from the release of SYSRESET to the turn on of the CPU_ACTIVE LED using a user level program named ONLED. The ONLED program shall be the last module loaded into RAM and executed using opexec or a startup file.

9.2.7.3.3 Startup Procedure

The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo shall operate as follows:

1. Sysgo shall set the execution directory to /f0wp/CMDS
2. Sysgo shall check if the backspace key (0x08) is being received on /sp4 (c50j). If received, Sysgo shall:
   a. Fork a shell with no arguments on /sp4 using the current directory.
   b. Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo shall fork another shell with no arguments on /sp4. Unless Sysgo dies, a shell shall always be provided on /sp4.
3. If the backspace key was not received, Sysgo shall check for the presence of a Datakey. If present and valid (Datakey Header Version 2 or greater), Sysgo shall check the Startup Override Byte in the Datakey header.

   If Startup Override is 0x01, Sysgo shall:

   a. Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header shall be a 2-byte value indicating the length of the script. The script shall immediately follow the length value, and shall be stored as ASCII text.
   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

   If Startup Override is 0x02, Sysgo shall:

a. Fork an executable module stored on the Datakey immediately following the header.

b. If there is any error loading or forking the module, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking the module, Sysgo shall then exit without forking a shell.

4. If the backspace key was not received and Startup Override Byte is 0xFF:

   a. Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.

   b. If there is any error loading or forking OPEXEC, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking OPEXEC, Sysgo shall then exit without forking a shell.

5. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC file:

   a. Sysgo shall fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.

   b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

6. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC and no startup file:

   a. Sysgo shall fork a shell as described in step 2.

9.2.7.3.4 Short Out

A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. ACFAIL/POWER DOWN transitions shall generate an interrupt. The interrupt shall update an OS-9 event named "ACFAIL". The "ACFAIL" event shall set a value 1 indicating an ACFAIL condition occurred for the DOWN transition and set 0 indicating non-ACFAIL condition for the HIGH transition. The IRQ7 and auto-vector 31(7) shall not be used to update the "ACFAIL" event.

In addition, the ACFAIL condition shall generate the OS-9 auto-vector 30(6) interrupt service. Each interrupt service installed shall exit with the "Carry Bit" set allow OS9 to propagate the ACFAIL interrupt. The Contractor shall supply an interrupt handler at priority 255 that acknowledges and clears the interrupt.

Priority 1 shall be reserved for the OS-9 system.

9.2.7.3.5 Long Out

A Long Out is defined as ACFAIL transition to LOW follow by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

9.2.7.4 Error Handler

9.2.7.4.1 Initialization and Power-Up Test

A manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions. If used, the error report shall be stored in the file /r0/ErrorReport and shall not exceed 11kb in size.

9.2.7.5 Network Requirements

On the MODEL 2070-1E CPU module, an OS-9 SPF Ethernet hardware driver and descriptor for the 68360 (SCC1) shall be provided in the operating system Boot Image. The descriptor shall be named spqe0.

9.2.7.5.1 BOOTOBJS

The following OS-9 modules should be included in the /f0/CMDS/BOOTOBJS flash disk directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links:

1. Drivers and Descriptors for PPP.
2. Drivers and Descriptors for SLIP.
3. LAN Comm Pak modules: spenet, enet, spip, ip0, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0, spipcp, ipcp0, splcp, lcp0, sphdlc, hdlc0, spslip, sps10
4. Network modules pkman, pkdvr, pk, pks
5. Network Trap Handler: netdb_local, netdb_dns
6. NFS Modules: nfs, nfsnul and nfs_devices.

The PPP and SLIP descriptors shall have baud rates and ports set as follows and be stored in the /f0/CMDS/BOOTOBJS directory,

hdlc0 and spsl0 configured to use /sp1 and 38400 bps

hdlc1 and spsl1 configured to use /sp2 and 115200 bps

hdlc2 and spsl2 configured to use /sp3 and 115200 bps

hdlc3 and spsl3 configured to use /sp4 and 38400 bps

9.2.7.5.2 CMDS

The following Network utilities shall be included and shall reside in the /f0/CMDS directory as identified in this specification.

arp, dhcp, tftp, tftpd ,ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetdc, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, nfsd, mountd, and showmount.

9.2.7.5.3 Multi-user functionality

The boot image init module shall be configured with a “default directory name” as /f0wp. This will allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session.

The following OS-9 modules should be included in the operating system boot image for the implementation of multi-user mode.

login, tsmon

9.2.7.5.4 Network Configuration

The modules inetdb, inetdb2 and rpcdb shall be generated by the make utility via the use of a makefile and the network configuration files residing the /f0/ETC directory. The generated inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The modules shall be configured with the network default values as defined in Section 9.2.6 (Data Key) via the interfaces.conf shell script.

9.2.7.5.5 Netcfg

A Utility Program named netcfg shall be provided that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid **(Datakey Header Version 2 or greater),**, netcfg shall set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line. The netcfg utility shall create a new inetdb, inetdb2 and rpcdb database module based on the Datakey network parameters or network parameters from the command line. The new inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The netcfg shall also allow the user to read, write and display network parameters to and from the Datakey via the command line prompt. If the Datakey is not present or invalid and the flag option is not “n” netcfg shall display an error and exit without altering the network configuration. The netcfg utility shall reside in /f0/CMDS.

Netcfg options:

a= Write IP Address in Datakey

m= Write Netmask Address in Datakey

g= Write Gateway Address in Datakey

If the checksum is incorrect when executing the –a, -m or –g option the following will occur:

1. The default Datakey data will be loaded.
2. The networking changes will be made to the default networking parameters.
3. The CRC will be recalculated.
4. The networking parameters will be written to the Datakey.

This option loads default networking parameters into the Datakey.

-d= Write Default Networking Parameters in the Datakey

This option will display the networking information contained in the Datakey.

-i= Reads Networking Parameters from the Datakey

This option will set the networking parameters permanently on the controller using values from the Datakey

-c= Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.

Normal operation of this option will be:

1. Read the Datakey networking parameters
2. Delete interfaces.conf and routes.conf from /f0/etc
3. Write new interfaces.conf and routes.conf in /f0/etc.
4. Execute idbgen to create new inetdb and inetdb2
5. Executes rpcdbgen to create a new rpcdb
6. Delete inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.
7. Relocate inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.

This option will display the current Controller Network Parameters such as the IP Address, Netmask and Gateway. This requires the network Stack to be initialized.

-r= Reads current Networking Configuration.

This option will set the networking parameters dynamically on the controller using values from the Datakey

-s= Sets Network Configuration Dynamically from the Datakey.

This option will set the networking parameters permanently on the controller using values from the command line. The option will do the same functions as option "c" with network parameters from the command line.

n= Set Controller Network Parameters without the Datakey

The netcfg -n [opts] -t [opts] -w [opts] shall allow the user to permanently set the IP Address, Subnet Mask and Gateway of the Model 2070 Controller when executed by the user at the command line using parameters provided by the user at the command line.

Where opts may be IP Address in the format xxx.xxx.xxx.xxx, netmask in the format xxx.xxx.xxx.xxx and gateway as xxx.xxx.xxx.xxx.

Example, the following sets the IP Address, Netmask and Gateway permanently in the Model 2070 Controller to 10.20.70.51, 255.255.255.0 and 10.20.70.254:

netcfg -n 10.20.70.51 –t 255.255.255.0 – w 10.20.70.254

These options will display the help menu on how to use the netcfg utility.

h, ?, blank = displays the help menu

The help menu shall consist of the following:

Netcfg Usage:

netcfg [- a] [-m] [-g] [-n] [-d] [- i] [-r] [-s]

-a	follows Ip Address	; Write IP Address in Datakey
-m	follows Netmask	; Write Netmask Address in Datakey
-g	follows Gateway	; Write Gateway Address in Datakey

-d ;Write Default Networking Parameters in the Datakey

-i ;Reads Networking Parameters from the Datakey

-c ;Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.

-r ;Reads current Controller Networking Configuration.

-s ;Sets Network Configuration Dynamically from the Datakey.

-n <network parameters> ;Set Controller Network Parameters without Datakey

Example of option –n:
netcfg -n 10.20.70.51 –t 255.255.255.0 – w 10.20.70.254

See Section 9.2.6 for additional information.

9.2.7.5.6 ETC

A set of example configuration files consistent with the above networking modules shall be provided in the /f0/ETC directory. This directory shall contain the following text files.
hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf. makefile, nfs.map, nfsd.map

9.2.7.6 Standard Microware File System Configuration

9.2.7.6.1 Directories

The 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBJS, /f0/ETC and /f0/SYS directories shall be implemented. Execute permission shall be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBJS shall contain the modules as identified above and other customizable descriptors and modules. The /f0/SYS shall also contain the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf and loadnfs.

9.2.7.6.2 Password

The /f0/SYS shall contain a "password" file. The password file should follow Microware's password file format for the addition and configuration of multiuser functionality and password protection. A user name “super” with password as “user” shall be defined in the password file.
A Termcap text file shall be include in the /f0/SYS directory. This Termcap file shall contain description fields defining the capability names and values of the front panel DISPLAY.

9.2.7.6.3 utilities

The utilities tar, make, fixmod , mshell and vi shall be included in the /f0/CMDS directory.

9.2.7.6.4 Ver

A Ver module shall be provided as part of the OS-9 Image and shall allow access to Controller’s Manufacturer Name, Image Build Number, TEES Version, Image Build Date and CPU Type.

Ver options:
- -a Shows all information
- -b CPU Type
- -d Image Build Date
- -m Controller’s Manufacturer Name
- -t TEES Version
- -v Image Build Version Number
- -? Display Help

CPU Type shall display 2070-1A, 2070-1E or 2070-1C.
Image Build Date shall be in the form of mm/dd/yyyy
Manufacturer’s name shall be shown as one word only.

TEES Version shall be “TEES XXXX EY” where XXXX is the
is the year of the TEES and Y is any Errata if applicable.
Ver without an option shall be the same as Ver -a.

Ver –a shall display all information as shown by the following example:

2070 -1E
03/06/2008
Vendor Name
TEES 2008 E5 ; E5 Would be blank if there are no Erratas.
Build V01.6

The help menu shall consist of the following:

Ver Usage:

Ver [- a] [-b] [-d] [-m] [-t] [- v] [-?]

-a	Shows all information
-b	CPU Type
-d	Image Build Date
-m	Controller’s Manufacturer Name
-t	TEES Version
-v	Image Build Version Number
-?	Display Help

9.2.8 Model 2070-1C CPU Software

9.2.8.1 Operating System

The model 2070-1C CPU Module shall be supplied with Linux 2.6.18 kernel or later. Platform specific options shall be selected by the manufacturer based on the requirements of the MPC 82xx/ 83xx and the Model 2070-1C CPU options selected by the agency.

The yellow-highlighted items shall be the minimum Linux kernel configuration features that shall be included in the kernel build; others shall be included when possible:

```
#
# Automatically generated make menuconfig
# Linux kernel version: 2.6.18
# Tue Nov 7 11:57:18 2006
#
#
# Code maturity level options
#
CONFIG_BROKEN_ON_SMP=y
CONFIG_LOCK_KERNEL=y
CONFIG_INIT_ENV_ARG_LIMIT=32
```

```
#
# General setup
#
CONFIG_LOCALVERSION=""
CONFIG_SWAP=y
CONFIG_SYSVIPC=y
CONFIG_IKCONFIG=y
CONFIG_IKCONFIG_PROC=y
CONFIG_INITRAMFS_SOURCE=""
CONFIG_EMBEDDED=y
CONFIG_SYSCTL=y
CONFIG_HOTPLUG=y
CONFIG_PRINTK=y
CONFIG_BUG=y
CONFIG_ELF_CORE=y
CONFIG_BASE_FULL=y
CONFIG_FUTEX=y
CONFIG_EPOLL=y
CONFIG_SHMEM=y
CONFIG_VM_EVENT_COUNTERS=y
CONFIG_RT_MUTEXES=y
CONFIG_BASE_SMALL=0
CONFIG_SLOB=y

#
# Loadable module support
#
CONFIG_MODULES=y
CONFIG_MODULE_UNLOAD=y
CONFIG_MODVERSIONS=y
CONFIG_MODULE_SRCVERSION_ALL=y
CONFIG_KMOD=y


#
# Processor type and features
#

CONFIG_PREEMPT=y
CONFIG_PREEMPT_BKL=y



#
# Bus options (PCI, PCMCIA, EISA, MCA, ISA)
#
CONFIG_PCI=y
CONFIG_PCI_GOANY=y
CONFIG_PCI_BIOS=y
CONFIG_PCI_DIRECT=y

#
# Executable file formats
#
CONFIG_BINFMT_ELF=y
CONFIG_BINFMT_AOUT=m

#
# Networking
#
CONFIG_NET=y
```

```
#
# Networking options
#
CONFIG_PACKET=y
CONFIG_PACKET_MMAP=y
CONFIG_UNIX=y
CONFIG_INET=y
CONFIG_IP_MULTICAST=y
CONFIG_IP_FIB_HASH=y
CONFIG_IP_PNP=y
CONFIG_IP_PNP_DHCP=y
CONFIG_IP_PNP_BOOTP=y
CONFIG_IP_PNP_RARP=y
CONFIG_SYN_COOKIES=y
CONFIG_TCP_CONG_BIC=y

#
# IP: Virtual Server Configuration
#
CONFIG_IPV6=y
CONFIG_NETFILTER=y




#
# Device Drivers
#

#
# Generic Driver Options
#
CONFIG_STANDALONE=y
CONFIG_PREVENT_FIRMWARE_BUILD=y
CONFIG_FW_LOADER=m

#
# Block devices
#
CONFIG_BLK_DEV_FD=y
CONFIG_BLK_DEV_LOOP=y
CONFIG_BLK_DEV_NBD=m
CONFIG_BLK_DEV_RAM=y
CONFIG_BLK_DEV_RAM_COUNT=16
CONFIG_BLK_DEV_RAM_SIZE=4096
CONFIG_BLK_DEV_RAM_BLOCKSIZE=1024
CONFIG_BLK_DEV_INITRD=y


#
# SCSI device support
#
CONFIG_SCSI=y
CONFIG_SCSI_PROC_FS=y

#
# SCSI support type (disk, tape, CD-ROM)
#
CONFIG_BLK_DEV_SD=y
#
```

```
#
# Network device support
#
CONFIG_NETDEVICES=y
CONFIG_DUMMY=y
#
# Ethernet (10 or 100Mbit)
#
CONFIG_NET_ETHERNET=y
CONFIG_MII=y
#
# Wan interfaces
#
CONFIG_WAN=y
CONFIG_PPP=y
CONFIG_PPP_FILTER=y
CONFIG_PPP_ASYNC=y
CONFIG_PPP_SYNC_TTY=y
CONFIG_PPP_DEFLATE=y
CONFIG_PPP_BSDCOMP=y
CONFIG_SLIP=y
CONFIG_SLIP_COMPRESSED=y
CONFIG_SLIP_MODE_SLIP6=y
#
# Input device support
#
CONFIG_INPUT=y
#
# Serial drivers
#
#
# Non-8250 serial port support
#
CONFIG_UNIX98_PTYS=y
CONFIG_LEGACY_PTYS=y
CONFIG_LEGACY_PTY_COUNT=256

#
#
#
CONFIG_RTC=y
#
#
# I2C support
#
CONFIG_I2C=y
#
# I2C Algorithms
#
CONFIG_I2C_ALGOBIT=m
CONFIG_I2C_ALGOPCF=m
#
# SPI support
#
CONFIG_SPI=y
CONFIG_SPI_MASTER=y
#
# USB support
#
CONFIG_USB_ARCH_HAS_HCD=y
CONFIG_USB_ARCH_HAS_OHCI=y
CONFIG_USB_ARCH_HAS_EHCI=y
```

```
CONFIG_USB=y
#
# Miscellaneous USB options
#
CONFIG_USB_DEVICEFS=y

#
# NOTE: USB_STORAGE enables SCSI, and 'SCSI disk support'
#
# may also be needed; see USB_STORAGE Help for more information
#
CONFIG_USB_STORAGE=y
CONFIG_USB_STORAGE_FREECOM=y
CONFIG_USB_STORAGE_ISD200=y
CONFIG_USB_STORAGE_DPCM=y

#
# USB Input Devices
#
CONFIG_USB_HID=y
CONFIG_USB_HIDINPUT=y

#
#



#
# File systems
#
CONFIG_EXT2_FS=y
CONFIG_EXT3_FS=y
CONFIG_JBD=y
CONFIG_INOTIFY=y
CONFIG_INOTIFY_USER=y
CONFIG_DNOTIFY=y

#
# DOS/FAT/NT Filesystems
#
CONFIG_FAT_FS=y
CONFIG_MSDOS_FS=y
CONFIG_VFAT_FS=y
CONFIG_FAT_DEFAULT_CODEPAGE=437
CONFIG_FAT_DEFAULT_IOCHARSET="iso8859-1"
CONFIG_NTFS_FS=m
CONFIG_NTFS_RW=y

#
# Pseudo filesystems
#
CONFIG_PROC_FS=y
# CONFIG_PROC_KCORE is not set
CONFIG_SYSFS=y
CONFIG_TMPFS=y
CONFIG_RAMFS=y

#
# Miscellaneous filesystems
#

#
# Network File Systems
```

```
#
CONFIG_NFS_FS=y
CONFIG_NFS_V3=y
CONFIG_NFSD=y
CONFIG_NFSD_V3=y
CONFIG_NFSD_TCP=y
CONFIG_ROOT_NFS=y
CONFIG_LOCKD=y
CONFIG_LOCKD_V4=y
CONFIG_EXPORTFS=y
CONFIG_NFS_COMMON=y
CONFIG_SUNRPC=y


#
# Native Language Support
#
CONFIG_NLS=y
CONFIG_NLS_DEFAULT="iso8859-1"


#
# Kernel hacking
#
CONFIG_TRACE_IRQFLAGS_SUPPORT=y
# CONFIG_PRINTK_TIME is not set
# CONFIG_MAGIC_SYSRQ is not set
# CONFIG_UNUSED_SYMBOLS is not set
# CONFIG_DEBUG_KERNEL is not set
CONFIG_LOG_BUF_SHIFT=14
# CONFIG_DEBUG_BUGVERBOSE is not set
# CONFIG_DEBUG_FS is not set
# CONFIG_UNWIND_INFO is not set
CONFIG_EARLY_PRINTK=y
# CONFIG_DOUBLEFAULT is not set

#
# Security options
#
# CONFIG_KEYS is not set
# CONFIG_SECURITY is not set

#
# Cryptographic options
#
CONFIG_CRYPTO=y
CONFIG_CRYPTO_HMAC=y
CONFIG_CRYPTO_MD4=y
CONFIG_CRYPTO_MD5=y
CONFIG_CRYPTO_SHA1=y
CONFIG_CRYPTO_DES=y
CONFIG_CRYPTO_AES=y
CONFIG_CRYPTO_ARC4=y

#
# Library routines
#
CONFIG_CRC_CCITT=y
CONFIG_CRC32=y
CONFIG_ZLIB_INFLATE=y
CONFIG_ZLIB_DEFLATE=y
```

9.2.8.2 Linux Drivers

All Linux Drivers provided in the Model 2070-1C CPU shall be compliant to AASHTO, ITE and NEMA ATC Standard V. 5.2.b Annex B and as defined in these specifications. In case of conflict these specifications shall govern over ATC Standard V.5.2b.

9.2.8.2.1 GPIO

`The GPIO driver allows the user to control the CPU active LED, determine if the Datakey is present, reset peripheral devices, and power down peripheral devices.`

`open()`

The following dev entries shall exist:
/dev/datakeypresent
/dev/cpuactive
/dev/powerdown
/dev/cpureset

`read()`
int read(int filp, void *buf, int count);

This allows for reading the state of the power down pin and for reading the state of the whether the Datakey is inserted. The value passed in the count parameter must be 1 or no bytes will be read.

`write()`
int write(int filp, void *buf, int count);

Allows changing the state of the CPU Active LED and the CPU reset signal.
Writing a single nonzero character to the /dev/cpuactive device shall turn on the CPU active LED and writing zero will turn off the LED.

`close()`

Closes the file descriptor.

9.2.8.2.2 Timers

This driver provides an abstraction for controlling up to 16 timers with 100µs resolution simultaneously. A timer can be used to send a one-shot or periodic signal to a process. A timer can be used in a free running mode where the timer is either restarted (stopped and cleared), started (running), or stopped. When the timer device node is opened, a timer is assigned automatically to the caller if one is available, thus eliminating the need for user applications to know which timers the other applications are using to avoid collisions.

```
Supported Device File Operations:
      open();
```

close();
read();
ioctl();

open()

The dev entry for the timer driver shall be /dev/timers. When the device is opened, a timer is automatically assigned to the caller if there is one available; otherwise an error is returned to the caller.

close()

Closes the file descriptor and reinitializes the timer, making it available to be reused.

read()

A call to read with a count of at least 4 bytes will read a binary 32-bit unsigned integer containing the current value of the open timer.

ioctl()
ioctl(int *fd*, unsigned int *cmd*, unsigned long *params*);

This ioctl passes a parameter structure for the parameters. The structure used is defined as follows:

```
typedef struct {
u32 code;
u32 param1;
union {
      u32 param;
      void *pointer;
} param2;
} timing_params_t;
```

The ioctl supports getting and setting a timer status structure defined as follows:

```
typedef struct {
      u32 value;
      u32 mode;
      u32 signal;
      u32 period;
} Timer_status;
```

Command Definitions:
ATC_TIMER_GET_PARAMS
ATC_TIMER_SET_PARAMS

ATC_TIMER_GET_PARAMS

When this command is issued, a timing_params_t shall be passed as the parameter. The params.code value shall be set to ATC_TIMER_GET_STATUS, params.param2.pointer shall point to a Timer_status structure, and params.param1 shall be the number of bytes allocated for the Timer_status structure. The current timer status shall be copied into the location at params.param2.pointer or an error will be returned if an invalid length or invalid pointer was passed to the ioctl.

```
timing_params_t params;
```

Parameter Code Definitions:

```
ATC_TIMER_GET_STATUS

Example for retrieving timer configuration:

params.code = ATC_TIMER_GET_STATUS;
params.param1 = sizeof(Timer_status);
params.param2.pointer = &Timer_status;

ioctl(fd, ATC_TIMER_GET_PARAMS, &params);


Status data should be returned in the structure pointed to by
params.param2.pointer as follows:
```

params.	param2.pointer→value	// current timer value in µS x 100
params.	param2.pointer→mode	// ATC__TIMER_SIG if one-shot signal pending, ATC_TIMER_CYC if periodic signal pending, ATC_TIMER_START if free running, ATC_TIMER_STOP if not active ATC_TIMER_RESET if timer is reset ATC_TIMER_NULL when timer is first initialized
params.	param2.pointer→signal	// signal code pending if ATC_TIMER_SIG or ATC_TIMER_CYC, 0 otherwise
params.	param2.pointer→period	// timer period in µS x 100 if ATC_TIMER_SIG or ATC_TIMER_CYC and Maximum Timer Period if ATC_TIMER_START , 0 otherwise

The following values shall be returned when the timer is in the ATC_TIMER_NULL (Timer initialized) Mode:

Timer Mode =	ATC_TIMER_NULL
Timer Value =	0
Timer Period =	0
Timer Signal =	0

The following values shall be returned when the timer is in the ATC_TIMER_START Mode:

Timer Mode =	ATC_TIMER_START
Timer Value =	Running Timer Value
Timer Period =	Maximum Timer Period
Timer Signal =	0

The following values shall be returned when the timer is in the ATC_TIMER_STOP Mode:

Timer Mode =	ATC_TIMER_STOP
Timer Value =	Current Timer Value
Timer Period =	0
Timer Signal =	0

The following values shall be returned when the timer is in the ATC_TIMER_RESET Mode:

Timer Mode =	ATC_TIMER_RESET
Timer Value =	0
Timer Period =	0
Timer Signal =	0

ATC_TIMER_SET_PARAMS

This function sets the mode of the timer based on the parameter code value in the structure of type timing_params_t that is passed as the parameter. As an example in the explanation of the parameter code definitions, the following variable will be used:

timing_params_t params;

Parameter Code Definitions:
ATC_TIMER_SIG
ATC_TIMER_CYC
ATC_TIMER_START
ATC_TIMER_STOP
ATC_TIMER_RESET
ATC_TIMER_NULL

ATC_TIMER_SIG

This command sends a one-time signal to the caller process after a specified time.

Example to set up a one-time signal to be sent after 1/10 of a second:

```
      params.code = ATC_TIMER_SIG;
      params.param1 = SIGALRM;      // signal code
      params.param2 = 1000;         // 1/10 of a second period
      ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_CYC

This command sets up a one-shot signal to be sent to the caller process after a specified time. While in this mode, the current timer value can be read at any time by calling the read() function.

Example to set up cyclical signal to occur every 1/10 of a second:

```
      params.code = ATC_TIMER_CYC;
      params.param1 = SIGALRM;      // signal code
      params.param2 = 1000;         // 1/10 of a second period
      ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_START

This command starts the timer without clearing its value. The timer value will be incremented every 100us. The current value can be read by calling read() or by calling the ioctl with command ATC_TIMER_GET_PARAMS, and read the period member of the Timer_status structure.

Example:
```
params.code = ATC_TIMER_START;
      ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_STOP

This command stops the timer without clearing its value. The current value can still be read while the timer is stopped.

Example:
```
params.code = ATC_TIMER_STOP;
      ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_RESET

This command stops the timer and resets the timer value. The timer value will read as 0 when in reset state.

Example:
```
params.code = ATC_TIMER_RESET;
      ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

9.2.8.2.1 Time of Day

The Time of Day driver overrides the operating system internal time of day to utilize AC line sync pulses or square wave pulses from the RTC. The time source can be changed via an ioctl command.

Supported Device File Operations:
open();
close();
read();
write();
ioctl();

open()

The dev entry for the timer driver shall be /dev/tod. The device can be opened for read, write, or read/write.

close()

Closes the file descriptor.

read() / write()
int read(int *filp*, void **buf*, int *count*);
int write(int *filp*, void **buf*, int *count*);

Reads / Writes the current time of day value in the following format:
YYYYMMDDHHMMSSFFF
Y = year   M = month   D = day   H = hour   M = minute   S = second   F = fraction

The fractional field shall be a value from 0 to 127 in RTC Square Wave Mode and a value from 0 to 2 * AC Line Sync Frequency - 1 in AC Line Sync Mode.

If the *count* passed to the read() function is greater than 18, only 18 bytes will be read. A read always starts with the 4 byte year in ASCII decimal. If the count is less than 18, then read shall modify *count* bytes in *buf*.

If the *count* passed to write() is less than 17 or the data in *buf* is not in the proper format, then write shall return an error of EINVAL.

ioctl()
ioctl(int *fd*, unsigned int *cmd*, unsigned long *param*);

The ioctl function supports multiple different commands, each described separately.

Command Definitions:

```
      ATC_TOD_SET
      ATC_TOD_GET
      ATC_TOD_SET_TIMESRC
ATC_TOD_GET_TIMESRC
ATC_TOD_GET_INPUT_FREQ
ATC_TOD_REQUEST_TICK_SIG
ATC_TOD_CANCEL_TICK_SIG
ATC_TOD_REQUEST_ONCHANGE_SIG
ATC_TOD_CANCEL_ONCHANGE_SIG
ATC_DST_ENABLE
ATC_DST_DISABLE
      ATC_DST_SET_INFO
ATC_DST_GET_INFO
```

ATC_SET and ATC_GET

These commands get and set the time and time zone atomically. The parameter to both functions is the same and defined below:

Parameter Data:

```
typedef struct {
  struct timeval *tv;
  int *tzsec_offset;
  int *dst_offset;
} atc_time_tz_t
```

The ATC_SET command is only concerned with the *tv* and *tzsec_offset* parameters. If the *tv* member is non-zero and the command is ATC_SET, then the time is set according to the tv_sec and tv_usec members of the struct timeval *tv. Additionally if the *tzsec_offset* parameter is non-zero the time zone offset is also set. The ATC_GET command sets the data pointed to by the *tv, tzsec_offset,* and *dst_offset* for each of those members that are non-zero.

ATC_SET_TIMESRC and ATC_GET_TIMESRC

Parameter Definitions:

```
ATC_TIMESRC_LINESYNC
            ATC_TIMESRC_RTCSQWR
            ATC_TIMESRC_CRYSTAL
            ATC_TIMESRC_EXTERNAL1
            ATC_TIMESRC_EXTERNAL2
```

These commands get and set the time source. The time source may use AC line sync pulses or the RTC square wave output.

ATC_TOD_GET_INPUT_FREQ

This command gets the current frequency that is driving the time of day clock.

ATC_TOD_REQUEST_TICK_SIG

This command requests a signal to be sent at each tick of the time of day clock as long as the file device remains opened. The *param* value passed to ioctl is the signal number that should be sent to the calling process at each time of day clock tick.

`ATC_TOD_CANCEL_TICK_SIG`

This releases the signal from being sent when the time of day clock ticks. If the file device is closed, the signal is automatically released.

`ATC_TOD_REQUEST_ONCHANGE_SIG`

This command requests a signal to be sent each time the time of day clock is changed by more than one tick. The *param* value passed to ioctl is the signal number that should be sent to the calling process.

`ATC_TOD_CANCEL_ONCHANGE_SIG`

This releases the signal from being sent when the time of day is changed by more than one tick. If the file device is closed, the signal is automatically released.

ATC_SET_DST_INFO and ATC_GET_DST_INFO

These commands allow setting the daylight savings time information, which shall be used when daylight savings time is enabled.

Parameter Data:

```
       typedef struct dst_info {
         char type;
         union dst_types_u {
           struct dst_absolute_struct {
             int secs_from_epoch_to_transition;
             int seconds_to_adjust;
           } absolute;
           struct dst_generic_struct {
             char month;
             char dom_type;
             union dst_gen_dom_union {
               char dom;
               // ex: second Saturday of month
               // ex: first Sunday on or after oct. 9
                struct dst_gen1_struct {
                 char dow;  // day of week (sun-sat)
                 char occur;    // number of occurrences
                 char on_after_dom; // day of month
               } week_and_day;
               // ex: second to last Thursday of month
               // ex: first Sunday on or before oct. 9
               struct dst_gen2_struct {
                 char dow;  // day of week (sun-sat)
                 char occur;  // number of occurrences
                 char on_before_dom // day of month
               } reverse_occurances_of_day;
             } gendom;
             int seconds_to_adjust;
           } generic;
         } begin, end;
         unsigned char begin_has_occurred_flag;
         unsigned char end_has_occurred_flag
       } dst_info_t;
```

The daylight saving time information contains two identical unions named begin and end. The begin union contains the information necessary to determine when daylight saving should begin going into effect by adjusting the time, and end union contains the information necessary to determine when daylight saving should end by re-adjusting the time. The unions contain two structures named absolute and generic. The type member of the struct dst_info shall be 0 for absolute or 1 for generic. The absolute structure contains the exact date and time the beginning/ending adjustment should be made, and by how many seconds the time should be adjusted. The generic structure contains information that can be valid for a number of years, by containing the month in which the beginning/ending adjustment should be made and a union named gendom (short for generic day of month), that contains the information to determine the day of the month on which the beginning/ending adjustment will take place for any particular year. The information in the generic day of month union determines a particular day of the month by finding the specific day of the week that occurs a specific number of times before or after a specific day of the month. The dom_type member of the union dst_gen_dom_union shall be a 0, 1, or 2 determining whether the dom member, dst_gen1_struct member or dst_gen2_struct union member respectively is used. The dom, on_after_dom, and on_before_dom members specify a day of the month from 1 to 31 inclusive. The occur member of these structures shall be 1 or greater, determining the number of times the particular day of the week, in the dow member (0 – 6, 0 being Sunday) shall occur to determine the day of the month when the daylight saving adjustment shall take place.

ATC_DST_ENABLE and ATC_DST_DISABLE

These commands enable and disable daylight saving time to be in effect.

9.2.8.2.2 EEPROM

The EEPROM driver provides full capability for reading and writing to EEPROM.

Supported Device File Operations:
open();
close();
read();
write();
lseek();
ioctl();

open()

The dev entry for the host EEPROM shall be /dev/eeprom. The EEPROM can be opened for Read, Write, or Read/Write.

Examples:

```
fd = open("/dev/eeprom", O_RDONLY);
fd = open("/dev/eeprom", O_WRONLY);
fd = open("/dev/eeprom", O_RDWR);
```

close()

Closes the file descriptor.

read()
int read(int *filp*, void **buf*, int *count*);

Reads up to *count* bytes into *buf* and returns the number of bytes read. The read occurs at the current position within the device.

> **Note: The current position can be determined using the ioctl. The current position can be changed using the lseek() function.**

Possible Errors:
EIO if end of file condition has already been reached

write()
int write(int *filp*, void **buf*, int *count*);

Writes *count* bytes to the device at the current file position within the device. If all of the bytes specified by *count* cannot be written before the end of the device no bytes shall be written and an error shall be returned. The number of bytes written shall be returned. If the value returned is less than *count*, then the returned value of bytes were written correctly, but the remaining bytes contain errors. In this case it is necessary to try the write again for the remaining bytes or repeat the same write again until the number of bytes returned matches the *count*.

Possible Errors:
EIO if end of file condition would occur writing the number of bytes specified.

`lseek()`
lseek(int *fd*, int *pos*, int *type*);

Seeks to a specified position in the device. Both absolute and relative types of seeking are supported. If relative seeking is specified the *pos* value may be positive or negative. If absolute seeking is specified the file position is assigned to the *pos* value. If seeking outside the device size is attempted an error is returned and no change to the file position takes place.

`Type Definitions:`
`ATC_EEPROM_SEEK_ABS`
`ATC_EEPROM_SEEK_REL`

`ioctl()`
ioctl(int *fd*, unsigned int *cmd*, unsigned long *param*);

The ioctl function supports multiple different commands, each described separately.

`Command Definitions:`
    `ATC_EEPROM_GET_FILE_POS`
    `ATC_EEPROM_GET_DEVICE_SIZE`

`ATC_EEPROM_GET_FILE_POS`

Returns the current file position. The *param* value is ignored.

`ATC_EEPROM_GET_DEVICE_SIZE`

Returns the size of the EEPROM device in bytes. The *param* value is ignored.

9.2.8.2.3 Datakey

This driver provides full capability for manipulating Datakey devices. Datakeys of sizes as listed in Section 9.2.6 of these specifications shall be supported.

`Supported Device File Operations:`
`open();`
`close();`
`read();`
`write();`
`lseek();`

ioctl();

open()

The dev entry for the Datakey shall be /dev/datakey. The Datakey can be opened for Read, Write, or Read/Write.

Examples:

fd = open("/dev/datakey", O_RDONLY);
fd = open("/dev/datakey", O_WRONLY);
fd = open("/dev/datakey", O_RDWR);

read()
int read(int *filp*, void **buf*, int *count*);

Reads up to *count* bytes into *buf* and returns the number of bytes read. The read occurs at the current position within the device.

> **Note: The current position can be determined using the ioctl. The current position can be changed using the lseek() function.**

Possible Errors:
ENXIO if Datakey is not present
EBUSY if the signature changes
EIO if end of file condition has already been reached

write()
int write(int *filp*, void **buf*, int *count*);

Writes *count* bytes to the device at the current file position within the device. If all of the bytes specified by *count* cannot be written before the end of the device no bytes shall be written and an error shall be returned. The number of bytes written shall be returned. If the value returned is less than *count*, then the returned value of bytes were written correctly, but the remaining bytes contain errors. In this case it is necessary to try the write again for the remaining bytes or repeat the same write again until the number of bytes returned matches the *count*.

Possible Errors:
ENXIO if Datakey is not present
EBUSY if the device signature changes (ie. Someone switched devices really fast)
EIO if end of file condition would occur writing the number of bytes specified.

close()

Closes the file descriptor.

lseek()
lseek(int *fd*, int *pos*, int *type*);

Seeks to a specified position in the device. Both absolute and relative types of seeking are supported. If relative seeking is specified the *pos* value may be positive or negative. If absolute seeking is specified the file position is assigned to the *pos* value. If seeking outside the device size is attempted an error is returned and no change to the file position takes place.

Type Definitions:
ATC_DATAKEY_SEEK_ABS
ATC_DATAKEY_SEEK_REL

ioctl()
ioctl(int *fd*, unsigned int *cmd*, unsigned long *param*);

The ioctl function supports multiple different commands, each described separately. If the Datakey is not inserted ENXIO is returned as the error code.

Command Definitions:
- **ATC_DATAKEY_GET_FILE_POS**
- **ATC_DATAKEY_ERASE_ALL**
- **ATC_DATAKEY_ERASE_SECTOR**
- **ATC_DATAKEY_READ_PROTECT_BITS**
- **ATC_DATAKEY_WRITE_PROTECT_BITS**
- **ATC_DATAKEY_GET_DEVICE_SIZE**
- **ATC_DATAKEY_GET_SECTOR_SIZE**

ATC_DATAKEY_GET_FILE_POS

Returns the current file position. The *param* value is ignored.

ATC_DATAKEY_ERASE_ALL

Erases all data on the Datakey. The *param* value is ignored. The CPU active light blinks with high frequency during erasure. Always returns 0.

Note: When data is erased, all values are read as 0xFF.

ATC_DATAKEY_ERASE_SECTOR

Erases all data in the sector containing the address specified by *param*. The CPU active light blinks at high frequency during erasure. Returns 0 on success or EINVAL on invalid address. The sector size can be determined using the appropriate ioctl() in order to know what address ranges will be erased by this command.

ATC_DATAKEY_READ_PROTECT_BITS

Returns the value of the protect bits directly read from the Datakey. The data format will be in accordance with the datasheet for the Datakey being used (not the same for different device sizes). This function is provided so the user can ensure that the device is not protected. The *param* value is ignored.

ATC_DATAKEY_WRITE_PROTECT_BITS

Writes the value specified in *param* directly to the Datakey protection byte. The data format varies in accordance with the datasheet for the Datakey being used. This function is provided primarily so that the user can remove protection if writing is being prevented.

ATC_DATAKEY_GET_DEVICE_SIZE

Returns the size of the Datakey device in bytes. The *param* value is ignored.

ATC_DATAKEY_GET_SECTOR_SIZE

Returns the sector size of the Datakey in bytes. The *param* value is ignored.

9.2.8.2.4 Constants Defined by this specification

The content of atc_spxs.h is displayed on this page.

```
#ifndef __ATC_SPXS_H
#define __ATC_SPXS_H

#define ATC_SPXS_WRITE_CONFIG   0
#define ATC_SPXS_READ_CONFIG    1

#define ATC_SDLC                0
#define ATC_SYNC                1
#define ATC_HDLC                2

#define ATC_B1200               0
#define ATC_B2400               1
#define ATC_B4800               2
#define ATC_B9600               3
#define ATC_B19200              4
#define ATC_B38400              5
#define ATC_B57600              6
#define ATC_B76800              7
#define ATC_B115200             8
#define ATC_B153600             9
#define ATC_B614400             10
const int ATC_B[] = { 1200, 2400, 4800, 9600, 19200, 38400,
                      57600, 76800, 115200, 153600, 614400 };

#define ATC_CLK_INTERNAL        0
#define ATC_CLK_EXTERNAL        1

#define ATC_GATED               0
#define ATC_CONTINUOUS          1

typedef struct atc_spcx_config_t {
    unsigned char protocol;
    unsigned char baud;
    unsigned char transmit_clock_source;
    unsigned char transmit_clock_mode;
} atc_spxs_config;

#endif
```

The content of atc.h is displayed on the following two pages.

```
#ifndef __ATC_H
#define __ATC_H

// Device File Names
#define ATC_HOST_EEPROM_DEV "/dev/eeprom"
#define ATC_ENGINE_EEPROM_DEV "/dev/engine_eeprom"
#define ATC_DATAKEY_DEV "/dev/datakey"
#define ATC_GPIO_POWERDOWN_DEV "/dev/powerdown"
#define ATC_GPIO_DATAKEY_DEV "/dev/datakeypresent"
#define ATC_GPIO_CPUACTIVE_DEV "/dev/cpuactive"
#define ATC_GPIO_CPURESET_DEV "/dev/cpureset"
#define ATC_TIMING_TOD_DEV "/dev/tod"
#define ATC_TIMING_TIMERS_DEV "/dev/timers"

#define ATC_SP1 "/dev/sp1"
#define ATC_SP2 "/dev/sp2"
#define ATC_SP3 "/dev/sp3"
#define ATC_SP4 "/dev/sp4"
#define ATC_SP5 "/dev/sp5"
#define ATC_SP6 "/dev/sp6"
#define ATC_SP8 "/dev/sp8"

#define ATC_SP1S "/dev/sp1s"
#define ATC_SP2S "/dev/sp2s"
#define ATC_SP3S "/dev/sp3s"
#define ATC_SP4S "/dev/sp4s"
#define ATC_SP5S "/dev/sp5s"
#define ATC_SP6S "/dev/sp6s"
#define ATC_SP8S "/dev/sp8s"

// DATAKEY IOCTL CONSTANTS
#define ATC_DATAKEY_GET_FILE_POS 3
#define ATC_DATAKEY_ERASE_ALL 6
#define ATC_DATAKEY_ERASE_SECTOR 7
#define ATC_DATAKEY_READ_PROTECT_BITS 8
#define ATC_DATAKEY_WRITE_PROTECT_BITS 9
#define ATC_DATAKEY_GET_DEVICE_SIZE 10
#define ATC_DATAKEY_GET_SECTOR_SIZE 11

// DATAKEY LSEEK CONSTANTS
#define ATC_DATAKEY_SEEK_REL 0
#define ATC_DATAKEY_SEEK_ABS 1

// EEPROM IOCTL CONSTANTS
#define ATC_EEPROM_GET_FILE_POS 3
#define ATC_EEPROM_GET_DEVICE_SIZE 10

// EEPROM LSEEK CONSTANTS
#define ATC_EEPROM_SEEK_REL 0
#define ATC_EEPROM_SEEK_ABS 1

// Time of Day driver Definitions
#define ATC_TOD_SET_TIMESRC 1
#define ATC_TOD_GET_TIMESRC 2
#define ATC_TOD_GET_INPUT_FREQ 3
```

```
#define ATC_TOD_REQUEST_TICK_SIGNAL 5
#define ATC_TOD_CANCEL_TICK_SIGNAL 6
#define ATC_TOD_DST_ENABLE 10
#define ATC_TOD_DST_DISABLE 11
#define ATC_TOD_DST_SETINFO 12
#define ATC_TOD_DST_GETINFO 13

// TIMING Driver Definitions
#define ATC_TIMER_GET_STATUS     0x1C
#define ATC_TIMER_NULL      0x0000  // When timer is initialized
#define ATC_TIMER_SIG       0x1000  // If one-shot signal is
pending */
#define ATC_TIMER_CYC       0x1001  // If periodic signal is
pending */
#define ATC_TIMER_START     0x1002  // If free running
#define ATC_TIMER_STOP      0x1003  // If not active
#define ATC_TIMER_RESET     0x1004  // If timer is reset

typedef struct
{
     unsigned int value;
     unsigned int mode;
     unsigned int signal;
     unsigned int period;
} Timer_status;

typedef struct
{
     unsigned int code;
     unsigned int param1;

     union
     {
          unsigned int param;
          void __user *pointer;
     } param2;
} timing_params;

#define ATC_TIMER_SET_PARAMS     0
#define ATC_TIMER_GET_PARAMS     1

#define ATC_SET_TIMESRC 1
#define ATC_TIMESRC_LINESYNC 0
#define ATC_TIMESRC_RTCSQWR 1



typedef struct atc_datakey_t {
    unsigned int16 fcs;
    unsigned int8 type;
    unsigned int8 version;
    unsigned int32 latitude;
    unsigned int32 longitude;
    unsigned int16 id;
    unsigned int16 drop;
    unsigned int32 ipaddress;
```

```
    unsigned int32 subnet;
    unsigned int32 gataway;
} atc_datakey;

#endif
```

9.2.8.3 Linux Application Kernel

9.2.8.3.1 Boot Sysreset

The provided software shall boot Linux from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the following defaults:

SP 1 & 2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP 3S	614.4 Kbps
SP 4	38.4 Kbps, 8-bit word, 1 stop, no parity, no pause, x on and x off BOTH OFF
SP 5S	614.4 Kbps
SP 6	38.4 Kbps, 8-bit word, 1 stop and no parity

9.2.8.3.2 Hardware Initialization

The Engine Board low-level hardware and O/S software initialization shall be completed within a maximum of 4.5 seconds from the release of STARTUP/SYSRESET as shown in A9-17. This startup time shall be measured from the release of STARTUP/SYSRESET to the turn on of the ACTIVE LED using a user level program named ONLED.

9.2.8.3.3 Startup Procedure

The Linux boot image shall startup as described in the AASHTO, ITE and NEMA ATC Standard V. 5.2.b Section 5.3.5.1. The boot up process shall be completed within the time period specified in Section 9.2.8.3.2 of these specifications.

Linux startup shall be configured to auto run scripts or execute Linux binaries residing in the USB Memory upon power up with USB Memory inserted. If there is no USB Memory inserted in the Model 2070-1C Module, Linux shall boot normally as defined above.

9.2.8.4 Linux Utilities

The following Linux utilities shall be provided resident in the Model 2070-1C CPU Module:

Ver , fl, onled

A Ver utility shall be provide in the /bin directory and shall meet the requirement as defined in Section 9.2.7.6.4 of this specification and as applicable for the Linux OS.

Re-Flash (fl) utility shall be provided in the /bin directory and shall meet the requirements as defined in Section 9.2.9 of this specification and as applicable for the Linux OS.

ONLED (onled) program shall be provided in the /bin directory. The onled program shall be a Linux binary and shall toggle the ACTIVE LED when executed.

9.2.8.5 Linux Network Requirements

The following Network utilities not listed under FHS-2.3 shall be provided resident in the Model 2070-1C CPU Module:

vi, arp, telnet, ftp, ifconfig, netstat, ping, showmount, ntpdate, ntpq, ntptime ntp-wait, and rpcinfo

The Model 2070 -1C CPU shall have full support for NFS and shall have the following daemons resident:

rpc.mountd, and rpc.nfsd

The Model 2070 -1C CPU shall have full support for FTP and shall have the following daemons resident:

vsftpd

The Model 2070 -1C CPU shall have full support for NTP and shall have the following daemons resident:

ntpd and ntdpc

9.2.8.6 Linux File System Configuration

The Model 2070-1C CPU Module Linux File System Configuration shall meet the requirements and guidelines for files, directories and utility commands as per the Filesystem Hierarchy Standard (FHS-2.3) dated January 28, 2004.

9.2.9 Re-Flash Utility

A Utility Program shall be provided that would allow the user to upgrade (re-flash) the Boot Image for the Model 2070-1A and E CPU as defined in section 9.2.7 and the Linux Kernel as defined in Section 9.2.8 for the Model 2070-1C CPU. This utility shall provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer. The Utility Program shall provide the capability for the user to dynamically upgrade the Boot Image via the command prompt. The contractor shall also provide a copy in CD-ROM Memory of all files originally stored in the flash drive /f0 so that they can be reloaded as needed.

9.2.10 Communications Loading Test

The Model 2070 Controller using the Model 2070-1A and 1E CPU shall pass a Communications Loading Test consisting of Serial and Network Communications. The test shall run Sp1, Sp2, Sp3, and Sp8 at 9600 bytes per second in a continuous full duplex asynchronous/synchronous communications loop with the network stack initialized and a telnet session established for each port with standard out, in and standard error directed to the telnet session port. The test shall not exceed a maximum

CPU load of 30% during test duration of 96 hours for Model 2070 -1E Module. The controller using Model -1C Module shall have a maximum CPU load of 10% for the above test and shall meet all test requirements as defined in Section 9.1.1 of the ATC v.5.2.b.

9.2.11 Diagnostic Acceptance Test (DAT)

The standard Caltrans DAT Program shall be provided resident in the 2070 Unit as the application program.

9.2.12 QPL or Purchasing Agency

Source and object Software shall be provided to the QPL or Purchasing Agency on both document listing and CD-ROM Memory. It shall provide user descriptions of test logic and reports. The Agency shall possess non- exclusive rights to this program suite.

9.2.13 Deliverables

9.2.12.1 Copies Delivery

Two copies of the following items will be provided to the purchasing AGENCY on a CD disk readable by a PC compatible computer.

1. Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, shall be specified and provided. Written documentation of addresses shall be in PDF form and will have the file name of “Memory Map.pdf”
2. Copies of the vendor kernel, platform drivers and OS-9 utility executable modules.
3. Copy of all provided written manuals in PDF form.
4. RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures shall have the file name of “Reflash Utility Procedures.pdf”.

9.2.12.2 Software Delivery

All Linux Software, except for loadable modules, shall be compliant to the GPL license as published by the Free Software Foundation.

CHAPTER 9-SECTION 3
MODEL 2070-2 FIELD I/O MODULE (FI/O)

9.3.1 Model 2070-2A Module

The Model 2070-2A Model shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

9.3.2 Model 2070-2B Module

The Model **2070-2B** Model shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

9.3.3 Field I/O Controller Unit (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. Operational software necessary to meet housekeeping and functional requirements shall be provided resident in socked firmware.

9.3.4 Parallel I/O Ports

The I/O Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 µA or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground. The pull-up resistance shall not be less than 10K or more than 50K Ohms.

9.3.4.1 I/O Ports

The I/O Ports shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 Mega Ohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 µs when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 ±2 µs duration, ±300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

9.3.4.2 Output

Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a LOGIC "0" and retain that state until a new writing. The state of all output circuits at the time of POWER UP or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 µs of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

9.3.5 Other Module Circuit Functions

9.3.5.1 Maximum Capacitive Load

A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

9.3.5.2 External WDT "Muzzle" Shunt

An External WDT "Muzzle" Shunt shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output 39 (Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to Set Output Command. When the shunt is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.3.5.3 Watchdog Circuit

An FCU Watchdog Circuit shall be provided. It shall be enabled by the Filed I/O firmware at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

9.3.5.4 One KHz Reference

A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of ±0.01% (±0.1 counts per second).

9.3.5.5 32 Bit Millisecond Counter

A 32-bit Millisecond Counter (MC) shall be provided for "time stamping." Each 1 KHz reference interrupt shall increment the MC.

9.3.5.6 Power Up

At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit.

9.3.5.7 Logic Switch

A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. An LED shall be provided on the module front panel labeled "SP3 ON". If LED light is ON, SP3 is active and available at C12S.

9.3.6 Serial Communications/Logic Circuitry

9.3.6.1 System Serial Port 5 (SP5) EIA 485 Signal

System Serial Port 5 (SP5) EIA 485 signal Lines shall enter the Field I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

9.3.6.2 System Serial Port 3 (SP3) EIA 485 Signal

System Serial Port 3 (SP3) EIA 485 signal lines shall enter the Field I/O Module and be isolated, converted back to EIA 485 and then routed to Connector C12S.

9.3.6.3 Linesync and Power Down Lines

Linesync and Power Down Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

9.3.6.4 CPU_Reset and Power Up

CPU_Reset and Power Up (SysReset) Lines shall be isolated and "OR'd" to form NReset. NReset shall be used to reset the FCU and other module devices. NReset shall also, be converted to EIA 485, and then routed to Connector C12S.

9.3.6.5 Module 2070-2B

If the module is 2070-2B, routing to FCU doesn't apply.

9.3.6.6 Internal Isolation

Isolation is between internal +5DC / DCG#1 and +12 DC ISO/DCG#2. +12 DC ISO shall be used for board power and external logic.

9.3.7 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition ($xxxx FFFF - $xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU Module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer.

9.3.8 I/O Functions

9.3.8.1 Inputs

Input scanning shall begin at I0 (bit 0) and proceed to the highest input I63, ascending from lsb to msb in increasing input number. Each complete input scan shall finish within 100 µs. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms ±100 µs. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 µs of the completion of the input scan.

9.3.8.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	**Enabled**
On and off filter values shall be set to	5
Transition monitoring	Disabled (Timestamps are not logged)

9.3.8.3 Outpust

Simultaneous assertion of all outputs shall occur within 100 µs. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the Module Status Byte shall be updated to reflect the loss of communication from the CPU Module.

9.3.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module Field I/O frame protocol as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

9.3.8.4.1 Case A

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 µs after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall neither glitch nor change state unless configured to do so.

9.3.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. LINESYNC Interrupt - both the 0-1 and 1-0 transitions of the LINESYNC signal shall generate this interrupt. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds ($\geq$60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer ($\geq$500 consecutive millisecond interrupts).

9.3.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

For Transmission:

Generate the opening and closing flags
Generate the CRC value
Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
Provide zero bit insertion

For Receiving:

Detect the opening and closing flags
Provide address comparison, generating an interrupt for messages addressed to the Field I/O Module, and ignoring messages not addressed to the Field I/O Module
Strip out inserted zeros
Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
Generate an interrupt if an abort sequence is received

9.3.8.7 Communication Processing

This task shall be to process the command messages received from the CPU Module, prepare, and start the response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

9.3.8.8 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9.3.9 Data Communication Protocols

9.3.9.1 Communications Protocol

Protocol - All communications between the CPU Module and the Field I/O shall be SDLC-compatible command-response, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communications and if the command frame is incomplete or there is an error, no Field FI/O response shall be transmitted. The number of bytes of a command or response is dependent upon the Field I/O Module identification.

9.3.9.1.1 Frame Types

The frame type shall be determined by the value of the first byte of the message. The command frames type values 112 – 127 ($70 - $7F) and associated response frame type values 240 – 255 ($F0 - $FF) are allocated for Manufacturer diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types

Module Command	I/0 Module Response	Description	Minimum Message Time	Maximum Message Time
0-43	128-171	Reserved for NEMA TS-2		
44-48	172-176	Reserved		
49	177	Request Module Status	250 µs	275 µs
50	178	**MC Management**	222.5 µs	237.5 µs
51	179	Configure Inputs	344.5 µs	6.8750 µs
52	180	Poll Raw Input Data	317.5 µs	320 µs
53	181	Poll Filtered Input Data	317.5 µs	320 µs
54	182	Poll Input Transition Buffer	300 µs	10.25 µs
55	183	**Set Outputs**	405 µs	410 µs
56	184	Configure Input Tracking	340 µs	10.25 µs
57	185	Configure Complex Outputs	340 µs	6.875 µs
58	186	Reserved / Optional (Configure Watchdog)	222.5 µs	222.5 µs
59	187	Controller Identification	222.5 µs	222.5 µs
60	188	I/O Module Identification	222.5 µs	222.5 µs
61-62	189-190	Reserved (see Section 9.3.9.1.2)	---	---
63	191	Poll variable length raw input (see Section 9.3.9.1.2)	317.5 µs	320 µs
64	192	Variable length command outputs	405 µs	410 µs
65	193	Reserved (see Section 9.3.9.1.2)	---	---
67	195	Reserved (see Section 9.3.9.1.2)	---	---
68-111	196-239	Reserved	---	---
112-127	240-255	Manufacturer Diagnostics	---	---

9.3.9.1.2 ITS Cabinet Monitor

Messages 61/189, and 62/190, and 65/193 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (See Chapter 3). Message 63 /191 shall be the same as Message 52/180 except Byte 2 of Message 63 response shall denote the following number of input data bytes:

Message 64/192 shall be the same as Message 55/183 except Byte 2 of the Message 64 Command shall denote the number of output data bytes plus the following output control bytes:

9.3.9.2 Request Module Status

The Command shall be used to request FI/O Module status information response.

Command/response frames are as follows:

Request Module Status Command

Description	**Msb**							**lsb**	**Byte Number**
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	**Msb**							**Lsb**	**Byte Number**
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

9.3.9.2.1 Status Bits

The response Status Bits are defined as follows:

- P - Indicates FI/O hardware reset
- E - Indicates a communications loss of greater than 2 seconds
- M - Indicates an error with the MC interrupt
- L - Indicates an error in the LINESYNC
- W - Indicates that the FI/O has been reset by the Watchdog
- R - Indicates that the SCC Receive Error count byte has rolled over
- T - Indicates that the SCC Transmit Error count byte has rolled over
- K - Indicates the Datakey has failed or is not present

9.3.9.2.2 Request Module Status

Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When an SCC error count rolls over (255 - 0), its corresponding roll-over flag shall be set.

9.3.9.3 MC Management

MC Management frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

MC Management Command

Description	**msb**							**Lsb**	**Byte Number**
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1
New Timestamp MSB	x	x	x	x	x	x	x	x	Byte 2
New Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3
New Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 4
New Timestamp LSB	x	x	x	x	x	x	x	x	Byte 5

MC Management Response

Description	**msb**							**Lsb**	**Byte Number**
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

9.3.9.4 Configure Inputs Command

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	**msb**							**Lsb**	**Byte Number**
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n	Byte 2
Item # - Byte 1	E	Input Number							Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)								Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)								Byte 3(I-1)+5

Configure Inputs Response

Description	**msb**							**Lsb**	**Byte Number**
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	S	Byte 2

Block field definitions shall be as follows:

E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input

e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)

r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)

S - return status S = '0' on completion or '1' on error

9.3.9.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	**Msb**							**lsb**	**Byte Number**
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1

Poll Raw Input Data Response (2070-2A)

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Raw Input Data Response (2070-8 via 2070-2B)

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

9.3.9.6 Poll Filtered Input Data

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	**Msb**							**lsb**	**Byte Number**
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1

Poll Filter Input Data Response (2070-2A)

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x	Bytes 3 to 9
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 10
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12

Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Filter Input Data Response (2070-8 via 2070-2B)

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20

9.3.9.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 54)	0	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2

Input Transition Buffer Response

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 182)	1	0	1	1	0	1	1	0	Byte 1
Block Number	x	x	x	x	x	x	x	x	Byte 2
Number of Entries (n)	x	x	x	x	x	x	x	x	Byte 3
Item #	S	Input Number							Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G	Byte 3(n-1)+7
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+8
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+9
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+10
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 3(n-1)+11

The entry types are depicted as follows:

Input Transition Entry

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	x	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

MC Rollover Entry

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

9.3.9.7.1 Active Input

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

- S Indicates the state of the input after the transition
- C Indicates the 255 entry buffer limit has been exceeded
- F Indicates the transition buffer limit has been exceeded
- G Indicates the requested block number is out of monotonic increment sequence
- E Same block number requested, E is set in response

9.3.9.7.2 Block Number Byte

The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

9.3.9.8 Set Outputs

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to "1". If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set to "1". Loss of LINESYNC reference shall also be indicated in Module Status Response Frame. The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command (2070-2A)

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O63 Data	x	x	x	x	x	x	x	x	Bytes 3 to 9
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 10
Outputs O8 to O63 Control	x	x	x	x	x	x	x	x	Bytes 11 to 17

Set Outputs Command (2070-8 via 2070-2B)

Description	Msb							lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O103 Data	x	x	x	x	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	Byte 15
Outputs O8 to O103 Control	x	x	x	x	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	Msb							lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E	Byte 2

9.3.9.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to ‘1’ and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb							lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	E	Output Number							Byte 2(I-1)+3
Item # - Byte 2	I	Input Number							Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	msb							lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 6

9.3.9.9.1 Definitions are as follows:

E '1’ - Enable input tracking functions for this output
'0' - Disable input tracking functions for this output
I '1' - The output is OFF when input is ON, ON when input OFF
'0' - The output is ON when input is ON, OFF when input is OFF
V '1' - The max. number of 8 configurable outputs has been exceeded
'0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

9.3.9.9.2 Timestamp Value

The timestamp value shall be sampled prior to the response frame.

9.3.9.9.3 Outputs Tracks Inputs

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

9.3.9.9.4 Number of Item

The "Number of Item" field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message "V" bit set to 1. If an invalid output or input number is specified for a function, the FIOM software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

9.3.9.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	msb							lsb	Byte Number
(Type Number = 57)	0	0	1	1	1	0	0	1	Byte 1
Number of Items	Number of Items								Byte 2
Item # - Byte 1	0	Output Number							Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)								Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)								Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)								Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)								Byte 7(I-1)+7
Item # - Byte 6	0	Input Number							Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	x	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	x	x	x	x	x	Byte 4
Timestamp (NLSB)	x	x	x	x	x	x	x	x	Byte 5

Timestamp (LSB)	x	x	x	x	x	x	x	x	Byte 6

9.3.9.10.1 Bit Field

The bit fields of the command frame are defined as follows:

E	'1'	-	enable complex output function for this output
	'0'	-	disable complex output function for this output
J	'1'	-	During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
	'0'	-	During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.
			Output Number - 7-bit output number identifying outputs
			Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.
			Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.
F	'1'	-	The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
	'0'	-	The trigger or gate shall be derived from the raw input.
R	'1'	-	For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
	'0'	-	For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
			Input Number - 7-bit input number identifying inputs 0 Up.
P	'1'	-	The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
	'0'	-	The output is configured for continuous oscillation.
W	'1'	-	It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
	'0'	-	Operation shall begin within 2 ms of the command receipt.
G	'1'	-	Operation shall be gated active by the specified input.
	'0'	-	Gating is inactive.
L	'1'	-	The LINESYNC based clock shall be used for the time ticks.
	'0'	-	The MC shall be used for the time ticks.
V	'1'	-	Indicates maximum number of configurable outputs is exceeded.
	'0'	-	No error
			Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

9.3.9.10.2 Controlling Input Signals

Controlling input signals shall be sampled at least once per millisecond.

9.3.9.10.3 Number of Items

The "Number of Items" field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message "V" bit shall be set to 1. If an invalid output or input number (the "G" or "W" bits being set to 1 is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The "G" bit (gating) set to 1 takes precedence over the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a Complex Output is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation ("G" bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

9.3.9.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb							lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1
Timeout Value	x	x	x	x	x	x	x	x	Byte 2

Configure Watchdog Response

Description	msb							lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1
Status	0	0	0	0	0	0	0	Y	Byte 2

9.3.9.11.1 Timeout Value

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

9.3.9.11.2 Watchdog Timeout Value

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the "Y" bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

9.3.9.12 Controller Identification

This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit "K" shall be set and no interrogation shall take place. If an error occurs during the interrogation, Bit "K" shall be set. If "K" bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

Controller Identification Command

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 59)	0	0	1	1	1	0	1	1	Byte 1

Controller Identication Response

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1
Status	0	0	0	0	0	0	0	K	Byte 2
Datakey	x	x	x	x	x	x	x	x	Byte 3 to 130

9.3.9.13 Module Identification

The Field I/O Identification command frame shall be used to request the FI/O Identification. A value Response of "1" for the 2070-2A, "2" for the 2070-8, and "3" for 2070-2N. Response values 32 to 40 are reserved for the ITS Cabinet (See Chapter 3). The command and response frames are shown as follows:

I/O Module Identification Command

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1

I/O Module Identification Response

Description	**msb**							**lsb**	**Byte Number**
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1
FI/O ID byte	x	x	x	x	x	x	x	x	Byte 2

CHAPTER 9-SECTION 4
MODEL 2070-3 FRONT PANEL ASSEMBLY (FPA)

9.4.1 Model 2070-3 Front Panel Assembly

The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connectors (DB9 and RJ-45), CPU_ACTIVE LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A- FPA controller, two keyboards, AUX switch, alarm bell & Display A.
OPTION 3B - FPA controller, two keyboards, AUX switch, alarm bell & Display B.
OPTION 3C - System Serial Port 6 Lines, isolated and vectored to Connector C60P.
OPTION 3D– FPA controller, two keyboards, AUX switch, alarm bell & Display D

9.4.2 Keyboards

Two Keyboards shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 1.764 ounce and 3.527 ounce and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

9.4.3 CPU_ACTIVE LED Indicator

The cathode of the CPU_ACTIVE LED Indicator shall be electrically connected to the CPU_ACTIVE signal and shall be pulled up to +5 VDC.

9.4.4 Display Liquid Crystal Display (LCD)

The Display shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with minimum character dimensions of 0.197 in. wide by 0.411 in. high and an electro-luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 0.104 in. wide by 0.167 in. high and either LED or EL backlight. Display D shall have 16 lines of 40 characters each with minimum dimensions of 0.104 in wide by 0.167 in high and either LED or EL backlight.

9.4.4.1 Characters and Angles of Liquid Crystal Display (LCD)

Each character shall be composed of a 5x7 dot matrix with a underline row or a 5x8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90^{o}) viewing, ±35^{o} vertical, ±45^{o} horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

9.4.4.2 Backlight

The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

9.4.4.3 Cursor Display

Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

9.4.5 FPA Controller

The FPA Controller shall function as the Front Panel Device controller interfacing with the CPU Module.

9.4.5.1 FPA Reset

A FPA Reset Switch shall be provided on the Assembly PCB. The momentary Control switch shall be logic OR'd with the CPU_Reset Line, producing a FPA Reset Output. Upon FPA Reset being active or receipt of a valid Soft Reset display command, the following shall occur:

Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
Each special character shall be set to ASCII SPC (space).
The tab stops shall be set to columns 9, 17, 25, and 33.
The backlight timeout value shall be set to 6 (60 seconds).
The backlight shall be extinguished.
The display shall be cleared (all ASCII SPC).
The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware Reset Button is pushed. The string is " ESC [PU", hex value "1B 5B 50 55".

9.4.5.2 Key Press

When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

9.4.5.3 Auto Repeat

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

9.4.5.4 AUX

When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

9.4.5.5 Controller Circuitry

The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication command codes on Page A9-12. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

9.4.5.6 Character Overwrite

Character Overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

9.4.5.7 Auto Wrap

Auto-Wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

9.4.5.8 Cursor Positioning

Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

9.4.5.9 Blinking Characters

Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

9.4.5.10 Tab Stops

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

Tab stops shall be set based only upon the column (horizontal) position of the cursor; the row position shall be ignored. Each tab that is set shall apply to all rows of the display. In this way, tabs shall operate similarly to a typewriter or line printer. For example, if the cursor is positioned at column 21, row 3 when a Set Tab Stop command (ESC H) is received, a tab stop is placed at column 21 and applies to every row of the display. If the cursor is then positioned to column 21, row 5, and a Clear Tab Stop command (ESC[0g) is received, the tab stop on column 21 is removed and there will be no tab stop on any row of the display at that column position.

9.4.5.11 Auto Scroll

Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

9.4.5.12 Displayable Characters

Displayable characters shall be refreshed at least 20 times per second.

9.4.5.13 Display Back Light Illuminate

The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

9.4.5.14 Command Codes

The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

   Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.

P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)

Px: Display column number (1-40), using one ASCII character per digit without leading zero.

Py: Display line (1-4) one ASCII character

...: Continue the list in the same fashion

Values of 'h' ($68) and 'l' ($6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.
3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

9.4.5.15 Controller Circuit

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

C50 Enable Function

C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

9.4.6 Front Panel

The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB, for 350±100 ms upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

CHAPTER 9-SECTION 5
MODEL 2070-4 POWER SUPPLY MODULE

9.5.1 Model 2070-4 Power Supply Module

The Model 2070-4 Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

9.5.2 On/Off Power Switch

An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC and 12 VDC are within 5% and of their nominal levels.

9.5.3 Input Protection

Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 µH inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 µF capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

9.5.4 +5 VDC Standby Power

+5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 µA at a range of +5 to +2 VDC for over 600 minutes.

9.5.5 Monitor Circuitry

Monitor Circuitry shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

9.5.5.1 AC Fail/Power Down Output Lines

The AC Fail/Power Down Output Lines shall go Low (ground true) immediately upon Power Failure. The Lines shall transition to High within 50 ms after both Power Restoration and supply is fully recovered. The Lines shall be driven separately. The Sysreset/Powerup Output Lines shall transition to Low 525 +/-25 ms after AC Fail/Power Down transition to Low. The Lines shall transition to HIGH 225 +/- 25 ms after both Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

9.5.5.2 Monitor Circuitry

The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

9.5.5.3 60 Hz Square Wave Linesync

The 60 Hz Square Wave Linesync signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 ± 1% duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

9.5.5.4 Linesync

The Linesync shall continue until Sysreset transitions Low and begin then Sysreset transitions High.

9.5.6 Power Supply Requirements

Voltage	Minimum Load	Maximum Load	Load Reg.	Line Reg.	Ripple & Noise
+5 VDC	0.0 Amp	10.0 Amp	± 5%	± 1%	50mV P-P
+12 VDC Serial	0.0 Amp	0.5 Amp	± 5%	± 1%	50mV P-P
-12 VDC Serial	0.0 Amp	0.5 Amp	± 5%	± 1%	50mV P-P
+12 VDC	0.0 Amp	1.0 Amp	± 5%	± 1%	50mV P-P

9.5.6.1 Line / Load Regulation

Shall meet Line/Load Regulation for input voltage range of 90 to 135 VAC, minimum and maximum loads called out in the table including ripple and noise.

9.5.6.2 Efficiency

70 % minimum.

9.5.6.3 Ripple & noise

Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater.

9.5.6.4 Voltage Overshoot

No greater than 5 %, all outputs.

9.5.6.5 Over voltage Protection

130% Vout for all outputs.

9.5.6.6 Circuit Protection

Automatic recovery upon removal of fault.

9.5.6.7 Inrush Current

Cold Start Inrush shall be less than 25 Amperes at 115VAC.

9.5.6.8 Transient response

Output voltage back to within 1% in less than 500 µs on a 50% Load change. Peak transient not to exceed 5%.

9.5.6.9 Holdup Time

The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

9.5.6.10 Remote Sense

+5 VDC compensates 250 mV total line drop. Open sense load protection required.

CHAPTER 9-SECTION 6
UNIT CHASSIS AND MODEL 2070-5
VME CAGE ASSEMBLY

9.6.1 General

The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.6.2 Serial Motherboard

Serial Motherboard shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the Motherboard PCB (provide strain relief). Test points shall be provided on the FPA side of the Motherboard for PS2 lines. A wiring harness FP shall be provided, linking the Motherboard with the FPA.

9.6.3 Model 2070-5 VME Cage Assembly

MODEL 2070-5 VME Cage Assembly shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. The VME Cage shall conform to VME Standard IEEE P1014/D12 and ANSI/VITA 1-1994 for 3U Cage. All slot/connectors shall be A24: D16 Interface.

9.6.4 Model 2070-1A

The Model 2070 – 1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

CHAPTER 9-SECTION 7
MODEL 2070 UNIT DETAILS

CHAPTER 10
MODEL 2070 PERIPHERAL
EQUIPMENT SPECIFICATIONS

CHAPTER 10-SECTION 1
MODEL 2070-6 A & B ASYNC/MODEM SERIAL COMMUNICATION MODULES

10.1.1 Fuse Isolation

A fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use.

Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse allowed.

10.1.2 Half & Full Duplex Switch

A switch shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.1.3 Circuits

Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-6x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.1.4 Modem

Each circuit shall have a common power independent Modem with the following requirements:

Data Rate: Baud modulation of 300 to 1200 for Module 2070-6A and 0 to 9600 for Module 2070-6B.

Modulation: Phase coherent frequency shift keying (FSK).

Data Format: Asynchronous, serial by bit.

Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive): 2070-6A - 1.2 KHz MARK and 2.2 KHz SPACE, ±1% tolerance. 2070-6B - 11.2 KHz MARK and 17.6 KHz SPACE, ±1% tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & .4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.

Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A & 14.7 KHz for 2070-6B) continuous or switch selectable.

Receiver Input Sensitivity: 0 to -40 dB.

Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20 dB/octave, minimum active attenuation for all frequencies outside the operating band.

Clear-to-Send (CTS) Delay: 11 ±3 ms.

Receive Line Signal Detect Time: 8 ±2 ms mark frequency.

Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

Soft Carrier Turn Off Time: 10 ±2 ms (0.9 KHz for 2070-6A and 7.8 KHz for 2070-6B). When the RTS is unasserted, the carrier shall turn off or go to soft carrier frequency.

Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.

Transmit Noise: Less than -50 dB across 600-Ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.

Modem interface: EIA-232 Standards.

10.1.5 Enable/Disable Feature

The 2070-6x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

10.1.6 Hot Swappable

The 2070-6x module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

CHAPTER 10-SECTION 2
MODEL 2070-7A & 7B ASYNC / SYNC
SERIAL COMM MODULE

10.2.1 Circuits

Two opto-isolated independent circuits designated circuits #1 and circuits #2, shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (circuits #1 to SP1 [or SP3] and Connector C21S and circuits #2 to SP2 [or SP4] and Connector C22S). Line drivers/receivers shall be socket or surface mounted.

The 2070-7x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.2.2 2070 -7A

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

10.2.3 2070 - 7B

Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

10.2.4 LED Indicator

Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled according to function.

10.2.5 Enable/Disable Feature

The 2070-7x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

10.2.6 Hot Swappable

The 2070-7x module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

CHAPTER 10-SECTION 3
MODEL 2070-6D FIBER OPTIC MODULE

10.3.1 Model 2070-6D Fiber Optics Module

The Model 2070-6D Fiber Optics Module shall provide an RS232/485 Asynchronous communications channel. The FO Module shall be a Plug-in Card style version for the 2070 Controller. The Model 2070-6D Fiber Optics Module (FO Module) shall operate over Singlemode Fiber.

10.3.2 Mechanical/Electrical Requirements.

The Plug-in Card FO Module shall have a protective cover or enclosure.

The FO Modules card edge connector shall be fully compatible with the 2070 Controller's Modem card slot.

The Auxiliary Data port shall be a RJ45 connector.

The Serial Port shall be a RJ45 connector.

All DIP Switches shall be accessed externally without disassembly of the FO Module.

The FO Module shall be powered direct from the 2070 Controller's edge connector.

All electro/optical communications circuitry shall be implemented using digital electronics utilizing packetizing techniques, no analog circuitry or adjustable potentiometers is allowed.

10.3.3 FO Module Requirements

All Electro Optics shall be physically protected from external damage and contamination by isolating them from the FO Modules Optical Ports by means of internal replaceable mini patch-cords that connect between the Electro Optics and the Optical Bulkhead Adapters (FO Modules Optical Ports).

The FO Modules Optical Ports (Bulkhead Adapters) shall be metal and shall be ST style and interchangeable with SC and FC style connectors when required.

The Plug-in optical FO Module shall provide Optical Continuity between other FO Modules on either side should external power fail.

10.3.3.1 Network Topologies

The FO Module shall be capable of operating on Single Mode Fiber in all of the following Switch Selectable Topologies:

Self-Healing Fault Tolerant Dual Counter Rotating Rings.
Defined as 2 Fiber Rings (closed loop cable ring), one fiber transmitting data clockwise, the other fiber anti-clockwise. Every FO Module will have 4 fibers attached to it, the incoming cable utilizes R1/T2 fiber pair and the outgoing cable utilizes T1/R2 fiber pair. Should an optical communications failure occur, such as a

single or dual fiber cut or FO Module failure, the system will automatically fold back on both sides of the failure point to form a new ring and restore communications. The system shall automatically restore when there is no longer a failure point.

Single Ring.

Defined as a Single Fiber Ring (closed loop), only one fiber transmitting data clockwise. Every FO Module will have 2 fibers attached to it R1 & T1, the incoming cable utilizes R1 fiber and the outgoing cable utilizes the T1 fiber. Each fiber starts as transmit and ends as receive.

Daisy Chain.

Defined as an “open ended chain of FO Modules”. The designated Master, Auxiliary Master and Slave FO Modules may be placed anywhere in the Daisy Chain, i.e., at the beginning, at the end or anywhere in between.

The FO Module shall be immune to optical overloads thus requiring no optical attenuators.

The FO Modules optical output level shall be non-adjustable.

10.3.3.2 Modes of Operation

The FO Module shall support the following modes of operation:

Master

When the optical FO Module is set as a Master, the FO Module supervises the Slave FO Modules and provides an asynchronous, bi-directional communications channel between the Master and the Slave FO Modules.

Auxiliary Master, Co- or Remote Located Master (Disaster Recovery)

When set as an Auxiliary Master, the optical FO Module will monitor optical data transmissions from the Master, should the Master fail, the Auxiliary Master will automatically take over as a temporary Master. Control of the ring will be automatically transferred back to any optical FO Module that is designated as a Master.

Slave
When the optical FO Module is set as a Slave, the FO Module will provide repeater, drop and insert capabilities between the data ports and the optical transport layer.

Display

All FO Modules shall have a Dual Seven Segment Display that graphically indicates the switching status of the transport layer of the fiber system. Switch status information shall graphically show:

Normal Operation
Dual Ring Operation
Single Ring Operation
Daisy Chain Operation
All Optical Routing Conditions
Separate LOS Alarm indication for R1 or R2

10.3.3.3 Fiber Identification

The FO Module shall be capable of Fiber Identification by means of indicating numeral 1 or 2 on the Dual Seven Segment Display to identify which circuit the fiber belongs to.

10.3.3.4 Auxiliary Data Port

The FO Module shall have an Auxiliary Data Port with the following capabilities:

The Auxiliary Data Port shall be capable of being switched to operate as a **DCE** in parallel with the Card Edge Port; communications shall originate to and from the fiber.

The Auxiliary Data Port shall be capable of being switched to operate as a **DTE**. This permits any host attached to the card edge port to appear at the Auxiliary port as a DTE with full handshaking; communications shall originate from the card edge port to and from the auxiliary port and the fiber.

The Auxiliary Ports Carrier Detect (CD) shall be capable of being switched to operate in the following modes:

The Auxiliary Data Port is designed to emulate FSK FO Module handshaking

The Card Edge (EIA-485), Auxiliary Data Port (EIA-232) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200, 2400, 9600, 19.2Kbp/s, 38.4Kbt/s, 56Kbt/s and 115.2Kbp/s.

The RTS/CTS handshaking function shall be switch selectable:

Off position allows the FO Module to stream transmit data without RTS handshaking. On position requires RTS to be asserted to enable data transmission.

The Card edge and Auxiliary Data Ports shall have a switch selectable RTS to CTS Delay of 0ms and 8ms.

10.3.3.5 Anti-Streaming

The FO Module shall include a switch selectable Anti-Streaming (anti-babbling) logic control over electrical to optical signal transmission with a time out changeable by the user, the time-outs shall be switch selectable from 2, 4, 8, 16, 32 & 64 seconds, all times are additive to a max of 126 seconds.

The Anti-Streaming logic shall detect the presence of an RTS signal from the attached device. Should the transmission time from the attached device exceed the selected time, the Anti-Streaming logic will cause the CTS control line to go low, this signals the attached device to stop the transmitting data. At the same time the transmission path from the data port to the optical ring will be disconnected. The circuit will automatically reset should RTS go low and data stops babbling.

When the Anti-Streaming logic has automatically disabled the port it shall then turn on the Anti-Streaming Alarm (LED), this alarm is latched ON until manually reset.

10.3.4 Electro Optical Requirements

The FO Module Optical Transmitting Device
shall use a 1310nm Singlemode Laser.

Optical Budget

The FO Module shall support a minimum of 20dB Optical budget with a maximum of 1×10^{-9} Bit Error Rate (BER).

M.T.B.F.

Shall be in excess of 100, 000 Hrs.

Optical Ports

Optical Ports shall be Metal Bulkheads, ST style, optional SC or FC.

Data Interfaces

Card Edge	EIA-485
Front Panel Serial Port	EIA-232 (RJ45 EIA 561 Pin Out)
Auxiliary Data Port	EIA-232 (RJ45 EIA 561 Pin Out)

Switch Selections are as follows:

Battery	ON or OFF
Master or Slave	Selection
Auxiliary Master	ON or OFF
Ring Topologies	Single Ring Dual Counter Rotating Ring (Self Healing) Daisy Chain
RS232 or RS422	Selection
Baud Rates	1200, 2400, 9600, 38400, 5760, 115200 bps
Parity Selections	None, Odd, Even
RTS/CTS Handshaking	ON or OFF
RTS to CTS Delay Timing	0 or 8ms
Anti Streaming	ON or OFF

Anti-Streaming Delay Times	2, 4, 8, 16, 32 & 64 seconds or any addition.
Auxiliary Port	DCE or DTE Selection

Indicators shall be Super Bright LED

TX DATA	Green	Transmit EIA-232/485 Data
RX DATA	Green	Transmit EIA-232/485 Data
ANTI- STRM	Red	Anti- Streaming
RING STATUS DISPLAY	Red	Dual Seven Segment Display
PWR Fail	Red	Dual Seven Segment Display

10.3.5 Form Factor

See A10-3 for Details

10.3.6 Power Requirements

The power requirements of the FO Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.3.7 Environmental

The FO Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 4
MODEL 2070-FX NETWORK COMMUNICATIONS MODULE

10.4.1 Model 2070-Fx Network Module

The Model 2070-Fx Module shall provide 5 ports for Network Communications to from the Model 2070 Controller.

An integrated 5-Port Store-and-Forward Network Switch shall be used as the core for the Model 2070-Fx Module. A network port shall be used to route Ethernet Traffic across the Motherboard to the “A” Connector’s Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively. Two network ports shall be brought to RJ-45 Connectors on the Front Panel and two network ports shall routed to 100Base-FX modules.

The 10/100Base-FX Module outputs shall be optically linked through short patch cords (Mini Patch Cords) to ST connectors on the Front Panel. The 10/100Base-FX modules shall operate over Single Mode Fiber.

The Model 2070-Fx Module shall be a Plug-in Card style version for the 2070 Controller.

10.4.2 Mechanical/Electrical Requirements.

The Model 2070-Fx Modules card edge connector shall be fully compatible with the 2070 Controller’s Motherboard Ax Card Slots.

The Model 2070-Fx Module shall be powered direct from the 2070 Controller’s edge connector.

10.4.3 Model 2070-Fx Module Requirements

The 10/100Base-FX modules of the Model 2070-Fx Module shall be connected by means of internal replaceable Mini Patch-Cords that connects between the 10/100Base-FX modules and the Optical Bulkhead Adapters (Model 2070-Fx Module Ports).

Model 2070-Fx Modules Optical Ports (Bulkhead Adapters) shall be metal and shall be ST style and interchangeable with SC and FC style connectors when required.

10.4.4 Network Standards

The Model 2070-Fx Module shall meet the IEEE802.3 10Base-T, IEEE 802.3u, IEEE 802.3x, 100Base-TX, and 100Base-FX Standards.

The Model 2070-Fx Module shall have 10/100Base-TX auto-negotiation on all RJ-45 ports and Auto-negotiation 10/100Mbps connection speed and Half/Full-Duplex mode on all 10/100Baset-TX ports.

The Model 2070-Fx Module shall have MDIX for all 10/100Baset-TX ports.

10.4.5 Modes of Operation

The Model 2070-Fx Module shall have Half/Full-Duplex mode selection on the fiber ports.

10.4.6 Network Media Support

The Model 2070-Fx Module shall be configured as a Multiple Channel Media Converter to route network traffic between the Model 2070 CPU, Two RJ-45 Front Panel Connectors and the two 10/100Base-FX Front Panel Ports.

The Model 2070-Fx Module shall support the following Media:

100Base-FX: Single-Mode fiber optic cable 9/125 µm.

100Baset-TX: Cat. 5, EIA/TIA-568 100-Ohm UTP cable.

10.4.7 Electro Optical Requirements

The 10/100Base-FX Modules shall use a 1300nm Single Mode Lasers.

M.T.B.F.

Shall be in excess of 100, 000 Hrs.

Optical Ports

Optical Ports shall be Metal Bulkheads, ST style, optional SC or FC.

10.4.8 Form Factor

See A10-4 for Details

10.4.9 Power Requirements

The power requirements of the 2070-Fx Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.4.10 Environmental

The 2070-Fx Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 5
MODEL 2070-6W WIRELESS MODEM COMM MODULE

10.5.1 Model 2070-6W Wireless Modem

The Model 2070-6W Wireless Modem shall provide two EIA-485/ EIA-232 Asynchronous communications channels. The Model 2070-6W Wireless Modem shall be a 2070 plug-in module with EIA-232 activity LEDs on the front edge. The Model 2070-6W Wireless Modem shall convert EIA-485 data to frequency hopping spread spectrum data.

10.5.2 Circuits

Two circuits, designated Circuits #1 and Circuits #2, shall be provided. Both circuits functions shall be identical, except for Circuit #1 which shall be routed to a Spread Spectrum Radio and Circuit #2 shall routed directly to the front panel's DB-9 connector. Each circuit shall provide full isolation from the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The Model 2070-6W Wireless Modem's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.5.3 Mechanical/Electrical Requirements

The Model 2070-6W Wireless Modem shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-6W Wireless Modem shall be provided with LED indicators for as shown in details A10-5 of these specifications.

The User Serial port shall be a DB9 Female connector accessible from the front and shall be used to configure the Spread Spectrum Radio and as Serial Port Com2..

The Model 2070-6W Wireless Modem shall be powered direct from the 2070 Controller's edge connector.

The Model 2070-6W Wireless Modem shall have a MTBF of over 60,000 hours.

10.5.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200, 2400, 9600, 19.2Kbp/s, 38.4Kbt/s, 56Kbt/s and 115.2Kbp/s.

10.5.5 Local Mode

The Model 2070-6W Wireless Modem shall be provided with a switch allowing the user to switch Com 2 into local mode. Local mode shall allow the user to perform modem configuration on the Spread Spectrum Radio. On non-local mode, Com 2 shall meet the requirements as specified for the Model 2070-7A Module as specified elsewhere in these specifications.

10.5.6 Spread Spectrum Radio

The Model 2070-6W Wireless Modem shall meet the following Spread Spectrum Radio requirements:

Frequency Range	902-928 MHz
Output Power	1mW, 10mW,100mW,1000mW
Software Programmable	Yes
Min Hop Patterns	62
Number of RF Channels	139
RF Channel Spacing	200kHs
Error Checking	16Bit-CRC
Encryption	32 Bit
Receiver Sensitivity/BER	-110dBm @ 10-6 BER
System Gain	152 dBm
Antenna Port	RP TNC-F
Certification	FCC Approved
Operation Mode	Transceiver
Error Correction	Forward Error Correction
System Configuration	Point-to-Point, Point-to-Multipoint

10.5.7 Data Interfaces

Channel 1 and 2   Model 2070 Card Edge Connector

User Serial Port   EIA-232 (DB9 Female)

10.5.8 LED Indicators

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

Multiple Mini-LEDs indicating Field Strength.

10.5.9 Power Requirements

The power requirements of the Model 2070-6W Wireless Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.5.10 Environmental

The Model 2070-6W Wireless Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.5.11 Form Factor

See A10-5 Details

CHAPTER 10-SECTION 6
MODEL 2070-9A/B FSK/DIAL-UP MODEM COMM MODULES

10.6.1 2070-9A/B Modem

The Model 2070-9x Modem shall consist of a Dial-Up and an FSK Modem. The 9x Modem Module shall be a Plug-in Card style version for the 2070 Controller.

10.6.2 Dial-Up Modem

The Dial-Up Modem shall consist of a 33.6Kbps dial-up modem meeting the V.34 AT Command set standard. The Modem shall contain two RJ-11 connectors, one designated as the Line and the second as Phone. An internal speaker shall be provided as an indicator for phone call progress. The speaker shall be controlled through AT standard commands. Front Panel LED indicators shall also be provided as shown in the A10-6 of these specifications.

10.6.2.1 Modem default configuration

The Dial-Up Modem shall contain the following default configurations:

ACTIVE PROFILE:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:007
S08:002	S48:007
S09:006	S95:000
S10:014	

STORED PROFILE 0:
B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0

S00:001	S12:050
S02:043	S18:000
S06:002	S36:007
S07:050	S40:104
S08:002	S41:195
S09:006	S46:138
S10:014	S95:000

S11:095	

Profile 0 should be configured as shown above and default as the active profile on wake up. Factory default shall wake up at 2400 Baud, Parity 8, N, 1 and no handshaking.

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Dumb
2	"SMART Modem DB-9 Aux" Sel	DTE	DCE
3	RTS Overide	Normal	RTS High
4	"Modem /DB9 DTE Serial" Sel	Modem	DB9-DTE

All switches shall be OPEN as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity. In SMART Mode the user shall have the ability to set the baud rate, handshaking and parity.

10.6.2.2 Modulation

The Dial-Up Modem shall use Quadrature Amplitude Modulation and
Operate within the following frequencies:

Data Carrier 1800 ± 0.5 Hz
Calling Tone 1300 ± 10 Hz
Answering Tone 2100 ± 15 Hz

The Modem shall have Receiver Frequency Tolerance of ± 14 Hz

10.6.2.3 Modem Standards

The Dial-Up Modem shall be ITU V.90, V.34 and Rockwell V.FC compatible. It shall meet the standards:

V.90, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, V.21, Bell 212, Bell 103, V.33, V.17, V.29, V.27 ter, and V.21 Channel 2.

10.6.2.4 Data Rates

The Dial-Up Modem shall support the following data rates:

33.6Kbps, 31.3Kbps, 28.8Kpbs, 26.4Kbps, 24.0Kbps, 21.6Kbps, 19.2Kbps, 16.8Kbps, 14.4Kbps, 12.0Kbps, 9.6Kpbs, 7.2Kpbs, 4.8Kpbs, 2.4Kpbs, 1.2Kpbs, and 300 baud.

The Modem shall automatically select the best operating speed as indicated in Section 10.6.2.1 of these specifications.

10.6.2.5 Error Correction & Data Compression

The Modem shall use V.42 LAPM, MNP2-4 and MNP 10 for error correction and V.42 Bis, MNP 5 for Data Compression.

10.6.2.6 Tx/Rx Power Level

The transmit level shall be fixed at -11± 2 dB and the receiver shall have a S/N Ratio of -26 dB with a Dynamic Range of 12 dBm to -42 dBm.

The Ring detect Sensitivity shall be 38 VRMS.

10.6.2.7 Line Interface

The Dial-Up Modem shall have a Ring Equivalent of 1 Bel and a terminating Impedance of 600 Ohms. It shall have return loss of better than 14 dB.

10.6.3 FSK Modem

10.6.3.1 Fused Isolated +5 VDC

A fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use.
Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Reset-able Fuse allowed.

10.6.3.2 Half & Full Duplex Switch

A switch on for FSK modem shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.6.3.3 Modem

The FSK modem circuit shall have meet the requirements as listed in Section 10.1.4 for the corresponding match (6A/6B).

10.6.3.4 Enable/Disable Feature

The FSK modem shall provide circuitry to disable Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

10.6.4 Circuits

Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-9x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.6.5 Hot Swappable

The 2070-9x module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

10.6.6 Power Requirements

The power requirements of the Model 2070-9x Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.6.7 Environmental

The Model 2070-9x Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.6.8 Form Factor

See A10-6 for Details

CHAPTER 10-SECTION 7
MODEL 2070-6E SERIAL 2 NETWORK COMM MODULE

10.7.1 Model 2070-6E Serial 2 Network Module

The Model 2070-6E Serial 2 Network (S2NET) Module shall provide two EIA-485/ EIA-232 Asynchronous communications channels. The Model 2070-6E S2NET Module shall be a 2070 plug-in module with EIA-232 activity LEDs on the front edge. The Model 2070-6E S2NET Module shall communicate over standard IEEE 802.3 networks using both TCP (point-to-point) and UDP (point-to-multipoint) protocols.

10.7.2 Circuits

Two circuits, designated Circuits #1 and Circuits #2, shall be provided. Both circuits functions shall be identical, except for Circuit #1 which shall be routed to the terminal server and Circuit #2 shall routed directly to the front panel's DB-9 connector. Each circuit shall provide full isolation from the Model 2070 Motherboard.
Line drivers/receivers shall be socket or surface mounted.

The Model 2070-6E S2NET Module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.7.3 Mechanical/Electrical Requirements

The Model 2070-6E S2NET Module shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-6E S2NET Module shall be provided with LED indicators for 10/100 and Half/Full Duplex Network Communications.

The User Serial port shall be a DB9 Female connector accessible from the front.

The Network port shall be a RJ45 modular jack connector accessible from the front.
DIP switches shall be externally accessible.

The Model 2070-6E S2NET Module shall be powered direct from the 2070 Controller's edge connector.

10.7.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200, 2400, 9600, 19.2Kbp/s, 38.4Kbt/s, 56Kbt/s and 115.2Kbp/s.

The Model 2070-6E S2NET Module Network Interface shall meet IEEE 802.3 and ANSI 8802-3 Standards and support 10/100 Mbps.

10.7.5 Echo Mode

The Model 2070-6E S2NET Module shall provided with a switch allowing the user to switch module into Echo Mode. In Echo Mode communications from the external network shall be routed serially to the DB-9 on the front panel. An LED indicator shall be provided to indicate the Echo Mode communications.

10.7.6 Network Configuration

The Model 2070-6E S2NET Module shall support the following features:

Provide TCP and UDP over IP protocol communications.

Subnet masks for Class A, B, and C networks (see table below):

NETWORK CLASS	HOST BITS	Subnet Mask	Example IP Address
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100
C	8	255.255.255.0	192.168.0.100

Allow Manual or Automatic TCP/IP socket connections configuration.

Provide Telnet access for both configuration and communications.

Provide Dumb Terminal access using a User Serial port for configuring network parameters.

Provide the Ability to adjust packet size and packing algorithm.

The Model 2070-6E S2NET Module shall be provided with a Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and Serial Settings using a Web Browser.

10.7.7 Data Interfaces

Channel 1 and 2	Model 2070 Card Edge Connector
User Serial Port	EIA-232 (DB9 Female)
Ethernet Data Port	RJ45 EIA 568B Pin Out

10.7.8 LED Indicators

RTS Green or Red: DTE Request to Send

CTS Green or Red: Network Clear to Send

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

DCD Green or Red: Network Data

10.7.9 Power Requirements

The power requirements of the Model 2070-6E S2NET Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.7.10 Environmental

The Model 2070-6E S2NET Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.7.11 Form Factor

See A10-7 for Details

CHAPTER 10-SECTION 8
2070 COMM MODULE DETAILS

CHAPTER 11
2070 / NEMA STANDARD
CONTROLLER UNITS

CHAPTER 11-SECTION 1
NEMA 2070

11.1.1 2070 / NEMA Standard Controller Units

This specification covers two versions of 2070 / NEMA Standard Controller Units. The versions associate with NEMA TS1/TS2 Type 2 and NEMA TS2 Type 1 Standards. They are as follows:

Model 2070 (V or L) N1 Controller Unit (TS1/TS2 Type 2)
Model 2070 (V or L) N2 Controller Unit (TS2 Type-1)

11.1.2 N1 Unit Consisting

The Model 2070 (V or L) N1 Controller Unit consists of:

Unit Chassis

2070- 1A or 1B CPU Module
2070-2B Field I/O Module
2070-3B Front Panel Module
2070-4NA Power Supply Module
2070-5 VME Cage Assembly, if required)
2070-8 Field I/O Module

11.1.3 N2 Unit Consisting

The MODEL 2070 (V or L) N2 CONTROLLER UNIT consists of:

Unit Chassis

2070-1A or 1B CPU Module
2070-2N Field I/O Module
2070-3B Front Panel Module
2070-4N (A or B) Power Supply Module
2070-5 VME Cage Assembly, if required)

11.1.4 Address

The Serial Port 5 Frame Address for 2070-2N and 2070-8 shall be “20”.

CHAPTER 11-SECTION 2
2N FIELD IO MODULE

11.2.1 2070-2N Field I/O Module

The 2070-2N Field I/O Module provides a TS2 Type 1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor LOGIC Output via SP5 on output O78 (similar to the 2070-8) to the NEMA TS2 Malfunction Management Unit (MMU). The communications timeout operation shall function in a manner similar to the 2070-8 (see sections 11.4.11.6 and 11.4.11.7 for details)

11.2.2 Requirements Exceptions

The Module shall meet the 2070–2A Module Requirements with the following exceptions:

No C1, C11 and C12 Connectors on the front panel of the module

No 64 inputs / 64 outputs requirements

Serial Port 5 routed to the FCU MPU Device only

Serial Port 3 shall not have a disabling switch

No Watchdog output

No Muzzle Shunt

11.2.3 Types

The module shall be a 4X type board/front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a Port 1 DA-15S connector labeled as either “C15S” or “Port 1”. The Port 1 (C15S) connector shall be a 15 pin metal shell DA-15 connector with female contacts. The connector shall be equipped with latching blocks and shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1, or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent.

11.2.4 Power

Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle with equipment ground also connected to the face plate. Connector A shall intermate with a NEMA TS2 Type 1 (MS3106( )-18-1S) cable.

11.2.5 Isolation

The module shall isolate 2070 Serial Port 3 from the A3 Connector and reconvert the lines to external EIA 485 drivers/receivers which shall be terminated at C15S Connector. The Port shall be clocked at 153.6 Kbps.

11.2.6 FCU Output

An FCU output shall drive an open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 mA at 30 VDC.

11.2.7 Connectors A, C15S pin out and functions

Connectors A and C15S pin out and functions are as follows:

CONNECTOR A

Pin	Function	Pin	Function	Pin	Function
A.	AC Neutral	E.	NA	I.	NA
B.	NA	F.	Fault Monitor	J.	NA
C.	AC Line	G.	DCG #2		
D.	NA	H.	EG (Equip Ground)		

CONNECTOR C15S:

Pin	Function	Pin	Function	Pin	Function
1	SP3TXD+	6	DCG #2	11	SP3TXC-
2	DCG #2	7	SP3RXC+	12	EG (Equip Ground)
3	SP3TXC+	8	DCG #2	13	SP3RXD-
4	DCG #2	9	SP3TXD-	14	NA
5	SP3RXD+	10	Port 1 Disable	15	SP3RXC-

11.2.8 Serial Port 3

Serial Port 3 shall control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards. SP3DCD shall be allocated to Port 1 Disable where 0 VDC input on C15S pin 10 equals DCD inactive (False). SP3DCD shall be opto-isolated from Port 1 Disable.

CHAPTER 11-SECTION 3
4N (A OR B) POWER SUPPLY MODULE

11.3.1 2070-4N Power Supply Module

The 2070-4N Power Supply Module supports the NEMA TS 1 and TS2 Standards. The module is identical to the 2070-4A Power Supply Requirements except for the following:

The power cord shall have a 15 inch ± 1 inch length as measured from the panel to the plug tips.

The AC Power Fail voltage shall be 85VAC ±2VAC.

The AC Power Restore voltage shall be 90VAC ±2VAC.

The 2070-4N (A) power supply shall have proper marking Example “2070 4N (A)”. A permanent sticker shall be an acceptable marking method.

CHAPTER 11-SECTION 4
MODEL 2070- 8 FIELD I/O MODULE

11.4.1 Module Consisting

The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS shall be made of 0.06 in. minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

11.4.2 Module Front Panel

The Module Front Panel shall be furnished with the following:

1. ON/OFF POWER Switch mounted vertically with ON in the UP position.
2. LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 3% and the +24 VDC is within 8%.
3. Incoming VAC fuse protection.
4. Two DB-25S COMM connectors labeled "EX1" & "EX2."
5. Four NEMA Connectors A, B, C, & D.

11.4.3 Label

A permanent Label shall be affixed to the Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

11.4.4 Module Power Supply

A Module Power Supply shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

11.4.4.1 Input Protection

Specification 9.5.3 Input Protection

11.4.4.2 Power Supply Requirements

The Power Supply shall meet the specification as listed in Section 9.5.6 Power Supply Requirements except Spec 9.5.3.

11.4.4.3 Tolerances

DC Voltage tolerances shall be ±3% for 5 VDC and ±8% for 24 VDC.

11.4.5 Incoming AC Power

The supplied Incoming AC Power shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

11.4.6 Module PC Boards

All Module PC Boards shall be mounted vertically.

11.4.7 POWERDOWN, NRESET, and LINESYNC

POWERDOWN, NRESET, and LINESYNC are incoming EIA-485 differential signals and shall be routed to the module via C12S Connector. The state of the module output ports at the time of POWERDOWN transition to LOW State and until NRESET goes HIGH shall be an open circuit.

11.4.8 Requirements

The Module shall meet all requirements under CHAPTER 9 SECTION 3 with the following exceptions:

11.4.8.1 Parallel Ports

118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12, Ground False ("0") exceeds 16.0 VDC, and Ground True ("1") is less than 8.0 VDC.

11.4.8.2 Serial Communication Circuitry

The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. HAR 1 Harness shall be 23 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to SP5 being routed to the FCU Controller interface, the SP3 EIA-485 Signal lines shall be routed only to the EX1 Connector.

11.4.9 EIA-232 Serial Port

An EIA-232 Serial Port on the FCU shall be provided with baud rate selection by Shunt of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector. This hardware is provided for future expansion capability and its use/protocol is currently undefined.

11.4.10 HAR 2 Harness

A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces between the 2070 UNIT and the outside world. The two EG (Equipment Ground) lines within HAR 2 shall be connected between EX2 and the 2070-8 module chassis.

11.4.11 Fault and Voltage Monitor Circuitry

NEMA TS1 Controller Fault and Voltage Monitor functions (outputs to cabinet monitor) shall be provided.

11.4.11.1 OR Gates

Conceptually, two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (Fault Monitor) and gate 2 output shall be connected to Connector A, Pin C. Any False state input shall cause a gate output False (+24VDC) state.

11.4.11.2 FCU Output O78

The FCU output O78 shall normally change its state every 100 ms. A module Watchdog circuit shall monitor the output. No state change for 2 ±0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the Watchdog output shall return to TRUE (0 VDC) state.

11.4.11.3 Operation

The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (±0.25). If the voltage exceeds the limits, the circuit output shall generate a False output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

11.4.11.4 Microprocessor Output

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

11.4.11.5 Message Outputs

CPU Port 5 Set Output Command Message Outputs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

11.4.11.6 CPU / FCU Operations

CPU / FCU operation at POWER UP shall be as follows:

1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
2. CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and FCU responds to CPU with "E" bit reset.
3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
4. * If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
5. Performs items 2 & 3 above User Software.

11.4.11.7 CPU / FCU Communications

A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm. Loss Flag. FM and VM outputs shall be in FALSE state.

CHAPTER 11-SECTION 5
2070N1 DETAILS

***Notes: Module sheet metal tolerance shall be 0.015 inch or less.**

APPENDIX A
CHAPTER DETAILS

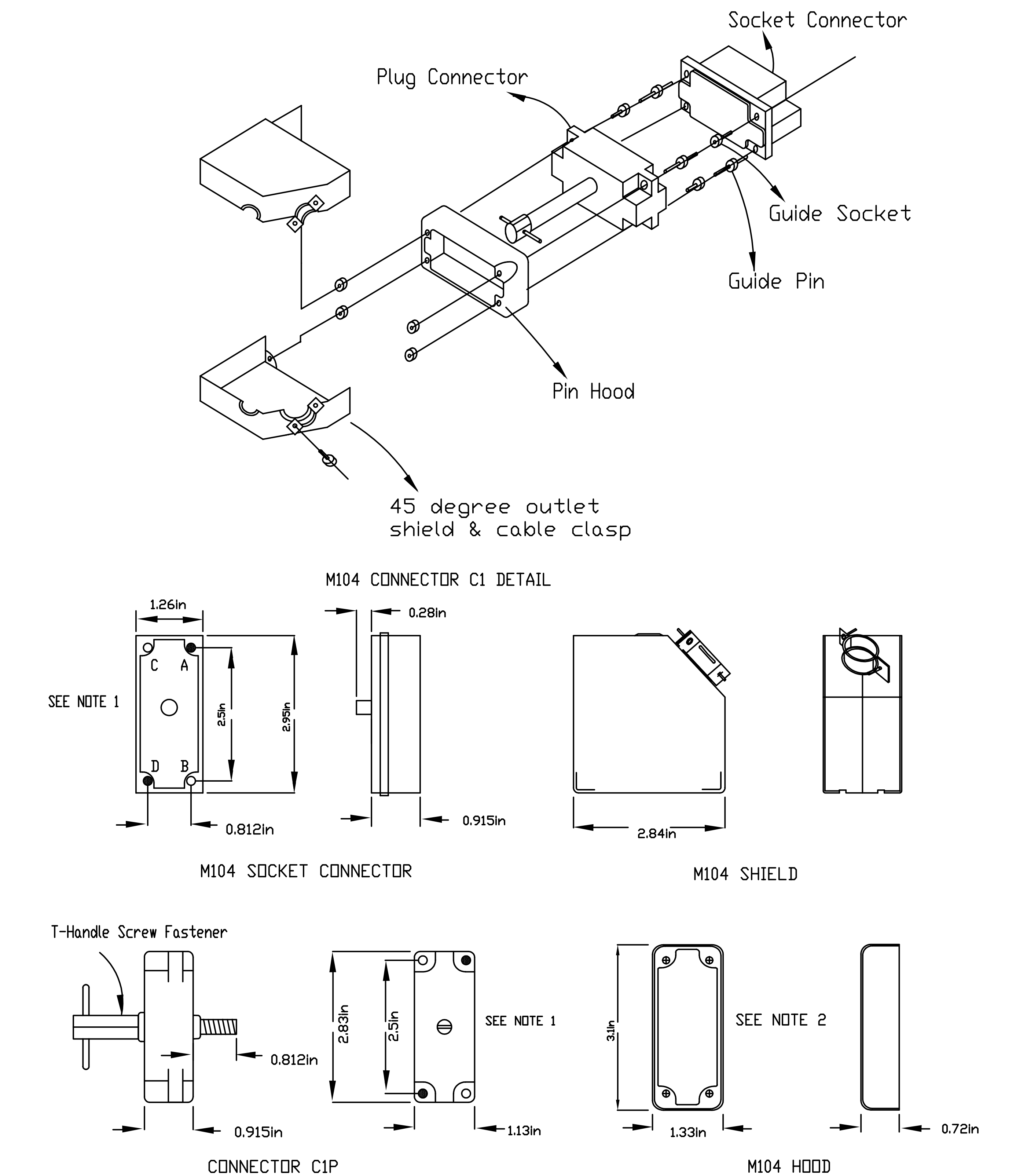
APPENDIX A1
CHAPTER 1 DETAILS

Section Notes:

M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 MegaOhms. The contacts shall be secured in the blocks with stainless steel springs.

M Type connector corner guides shall be stainless steel. The guide pins shall be 27.86 in length and the guide sockets shall be 15.66 in length.

Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated, heat stabilized and fire resistant.



NOTES:

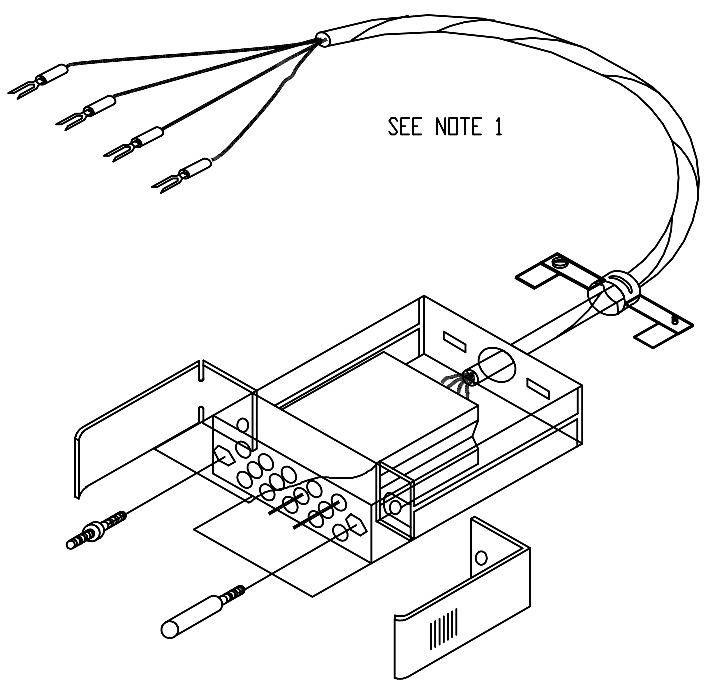
1. The darker circles denote guide pin location and the open circles are guide sockets.

2. Provide clearance for M104 plug with hood when mounting to it's socket.

TITLE:

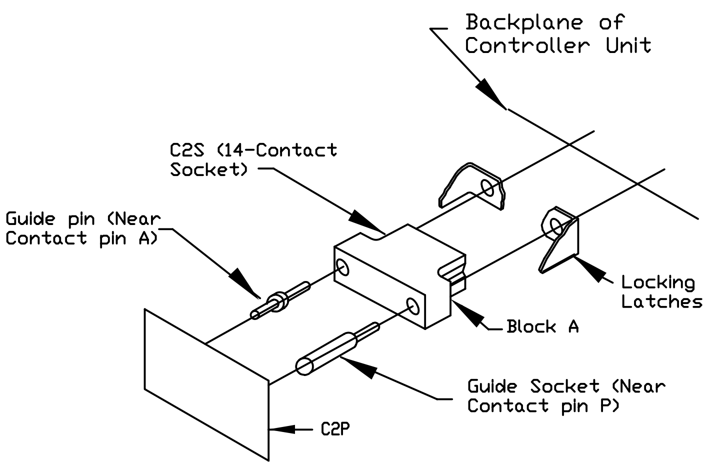
CONNECTOR DETAIL-M104

NO SCALE	A1-1
TEES 2008	

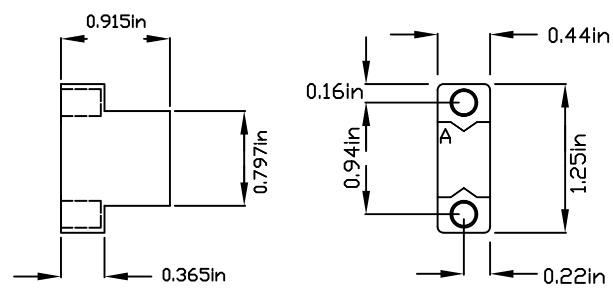


C2P MODEM INTERCONNECT HARNESS

C2P CONNECTOR ASSIGNMENT		
PIN	FUNCTION	WIRE COLOR
A	AUDIO IN	WHITE
B	AUDIO IN	BLACK
C	AUDIO OUT	RED
E	AUDIO OUT	GREEN



CONNECTOR C2 DETAIL

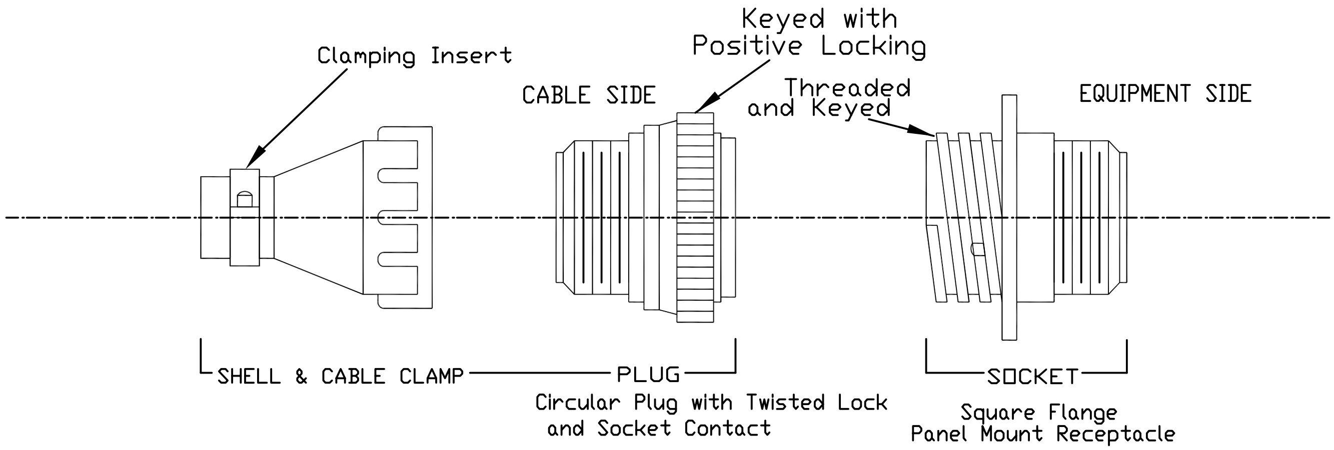


CONNECTOR C2S

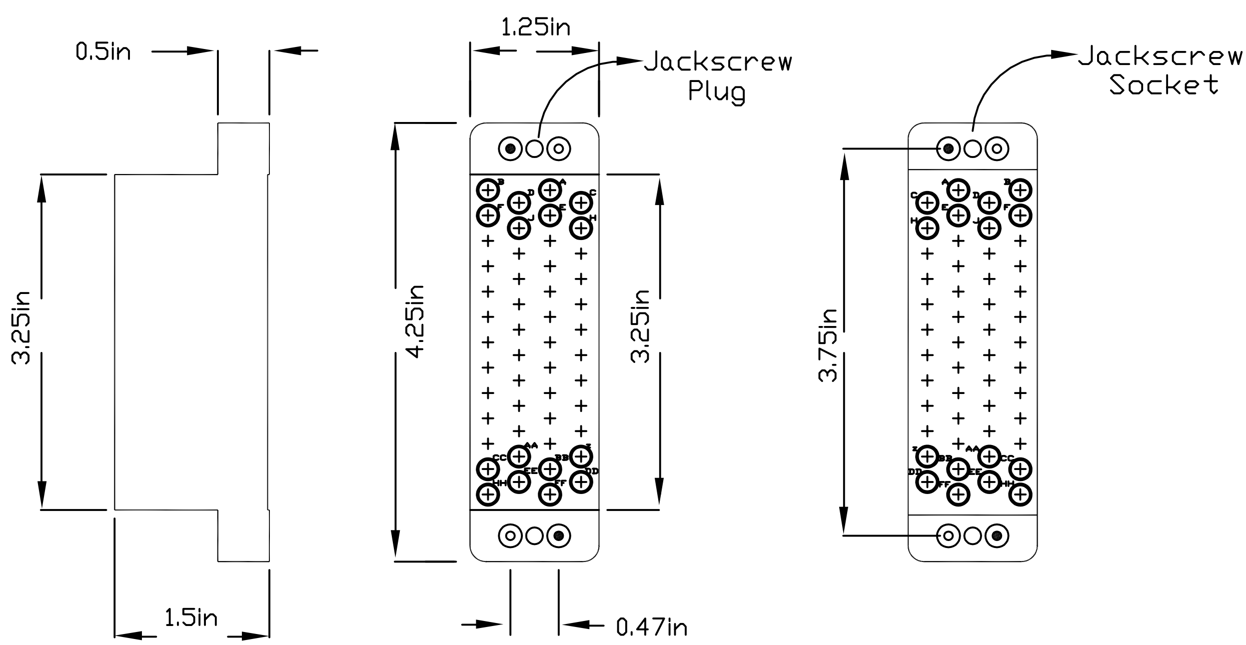
NOTES:

1. Cable length shall be 35.98in minimum. The cable shall be 2-pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.

TITLE: CONNECTOR DETAIL - M14	
NO SCALE	A1-2
TEES 2008	



PLASTIC CIRCULAR PLUG AND SOCKET CONNECTOR



CONNECTOR PIN ARRANGEMENT

NOTES:

1. Guide Pins & Sockets, and Jackscrews are centered symmetrical to connector.

2. Key: - socket
 - plug

TITLE: CONNECTOR DETAIL M50 & CIRCULAR PLASTIC CONNECTOR	
NO SCALE	A1-3
TEES 2008	

APPENDIX A2
CHAPTER 2 DETAILS

NOTES:

5. Program module' height and width dimensions are maximum.

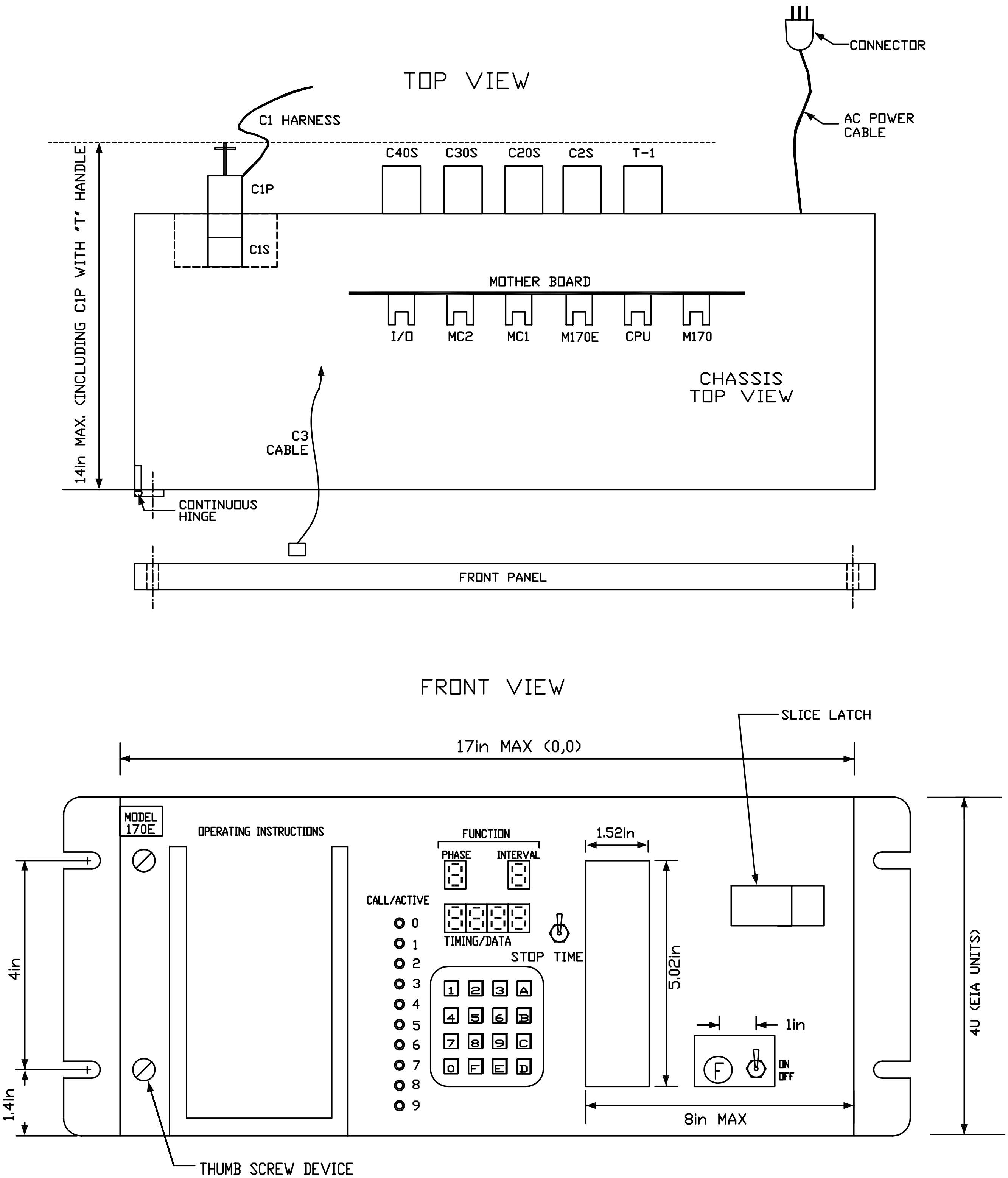
6. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.

7. All function under connector C2 & the terminal block T-1 are in reference to the MODEM

8. Detail Definitions:

BL = BLANKING
CC = CHARACTER CONTROL OR STROBE
CD = CARRIER DETECT
CH = CHARACTER
CTS = CLEAR TO SEND
DP = DECIMAL POINT
LS = LEAST SIGNIFICANT
MS = MOST SIGNIFICANT
NA = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
NLS = NEXT LEAST SIGNIFICANT
NMS = NEST MOST SIGNIFICANT
P&I = PHASE AND INTERVAL
RTS = REQUEST TO SEND

MODEL 170E CONTROLLER UNIT DIAGRAM

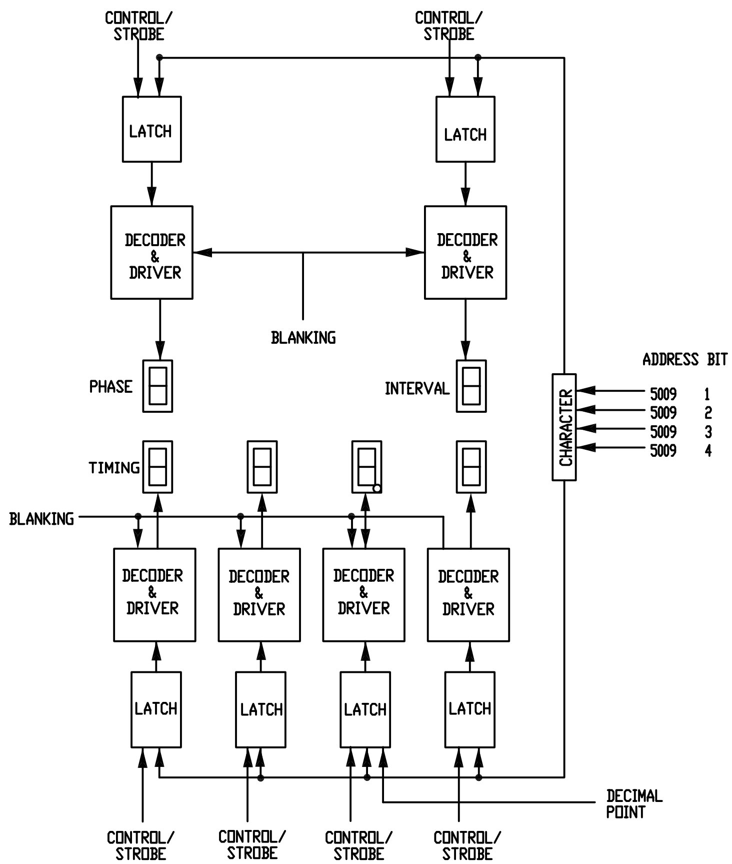


FRONT PANEL DISPLAY AND UNIT DETAIL

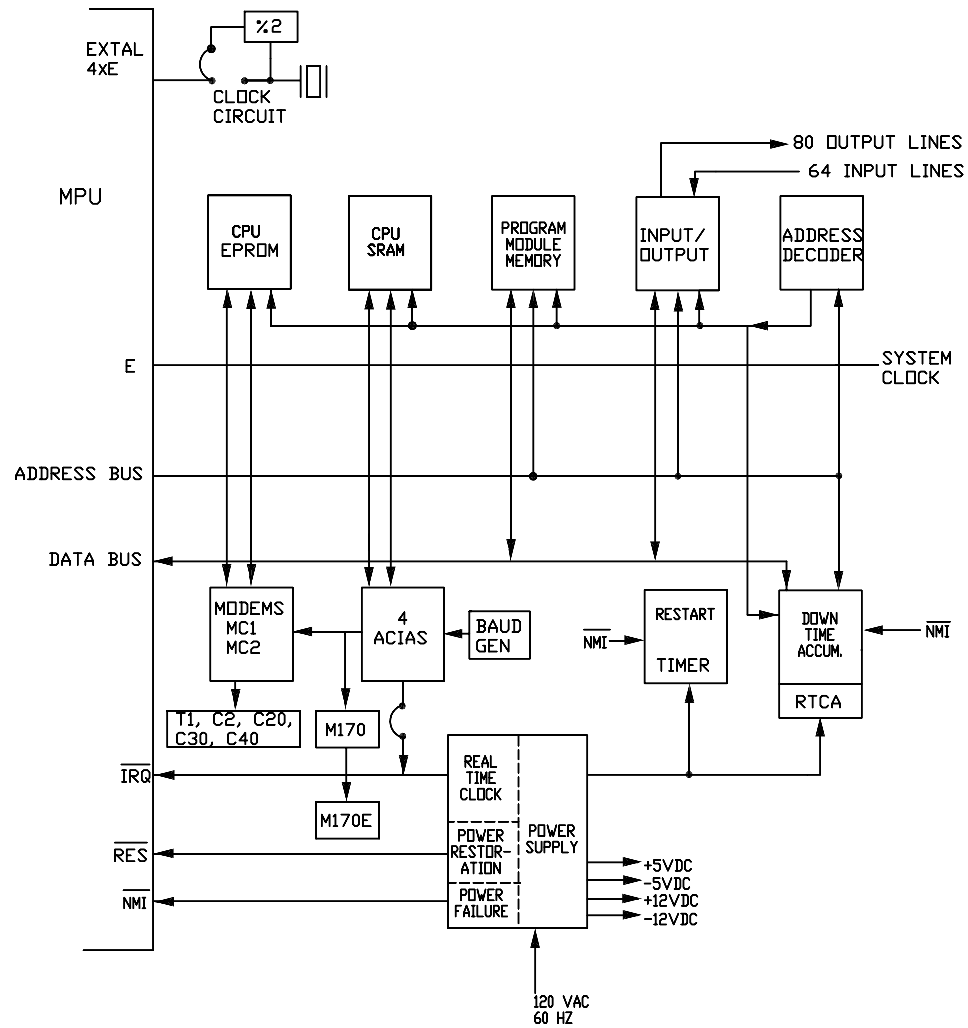
TITLE: MODEL 170E CONTROLLER UNIT DIAGRAM	
NO SCALE	A2-1
TEES 2008	

MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

FRONT PANEL DISPLAY BLOCK DIAGRAM



ORGANIZATION OF MODEL 170E CONTROLLER UNIT BLOCK DIAGRAM



TITLE: MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

NO SCALE

TEES 2008

A2-2

INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	INPUT PORT ADDRESS	BIT	CONNECTOR C1 C3 SOCKET CONTACTS	
5001	1	39	5005	1	67	
5001	2	40	5005	2	68	
5001	3	41	5005	3	69	
5001	4	42	5005	4	70	
5001	5	43	5005	5	71	
5001	6	44	5005	6	72	
5001	7	45	5005	7	73	
5001	8	46	5005	8	74	
5002	1	47	5006	1	75	
5002	2	48	5006	2	76	
5002	3	49	5006	3	77	
5002	4	50	5006	4	78	
5002	5	51	5006	5	79	
5002	6	52	5006	6	80	
5002	7	53	5006	7	81	
5002	8	54	5006	8	82	
5003	1	55	5007	1		KEYBOARD CONTROL
5003	2	56	5007	2		KEYBOARD CH LS
5003	3	57	5007	3		KEYBOARD CH NLS
5003	4	58	5007	4		KEYBOARD CH NMS
5003	5	59	5007	5		KEYBOARD CH MS
5003	6	60	5007	6		STOP TIMING
5003	7	61	5007	7		NA
5003	8	62	5007	8		NA
5004	1	NA	5008	1		NA
5004	2	NA	5008	2		NA
5004	3	NA	5008	3		NA
5004	4	NA	5008	4		NA
5004	5	63	5008	5		NA
5004	6	64	5008	6		NA
5004	7	65	5008	7		NA
5004	8	66	5008	8		NA

CONNECTOR C2 SOCKET ASSIGNMENT (C20, C30 & C40)

C2 SOCKET CONTACTS	FUNCTION	C2 SOCKET CONTACTS	FUNCTION
A	Audio IN	J	RTS
B	Audio IN	K	Data IN
C	Audio OUT	L	Data OUT
D	+5VDC	M	CTS
E	Audio OUT	N	DC GND
F	-5VDC	P	NA
H	CD	R	NA

TERMINAL BLOCK T-1 ASSIGNMENTS

1. Audio IN
2. Audio IN
3. CD
4. RTS
5. Data IN
6. CTS
7. Data Out
8. Audio Out
9. Audio Out
10 DC GND

TITLE: MODEL 170E INPUT ADDRESS	
NO SCALE	A2-3
TEES 2008	

OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	CONNECTOR C3
5001	1	2	5006	1	83	
5001	2	3	5006	2	84	
5001	3	4	5006	3	85	
5001	4	5	5006	4	86	
5001	5	6	5006	5	87	
5001	6	7	5006	6	88	
5001	7	8	5006	7	89	
5001	8	9	5006	8	90	
5002	1	10	5007	1	91	
5002	2	11	5007	2	93	
5002	3	12	5007	3	94	
5002	4	13	5007	4	95	
5002	5	15	5007	5	96	
5002	6	16	5007	6	97	
5002	7	17	5007	7	98	
5002	8	18	5007	8	99	
5003	1	19	5008	1		CC-PHASE
5003	2	20	5008	2		CC-INTERVAL
5003	3	21	5008	3		CC-TIMING LS
5003	4	22	5008	4		CC-TIMING NLS
5003	5	23	5008	5		CC-TIMING MLS
5003	6	24	5008	6		CC-TIMING MS
5003	7	25	5008	7		CALL LT 8
5003	8	26	5008	8		CALL LT 9
5004	1	27	5009	1		CH-LS
5004	2	28	5009	2		CH-NLS
5004	3	29	5009	3		CH-NMS
5004	4	30	5009	4		CH-MS
5004	5	31	5009	5		DP
5004	6	32	5009	6		BL-P&I
5004	7	33	5009	7		BL-TIMING
5004	8	34	5009	8		NA
5005	1	35	500A	1		CALL LT 0
5005	2	36	500A	2		CALL LT 1
5005	3	37	500A	3		CALL LT 2
5005	4	38	500A	4		CALL LT 3
5005	5	100	500A	5		CALL LT 4
5005	6	101	500A	6		CALL LT 5
5005	7	102	500A	7		CALL LT 6
5005	8	103	500A	8		CALL LT 7

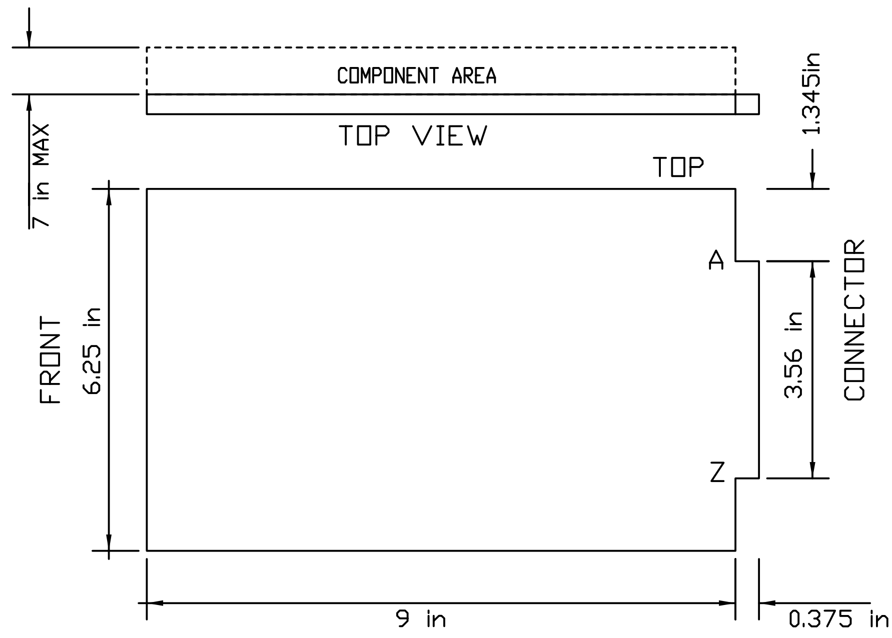
TITLE: OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 & C3

NO SCALE

TEES 2008

A2-4

MODEL 400 MODEM MODULE



MODEL 400 MODULE CONNECTOR ASSIGNMENT

COMPONENT SIDE

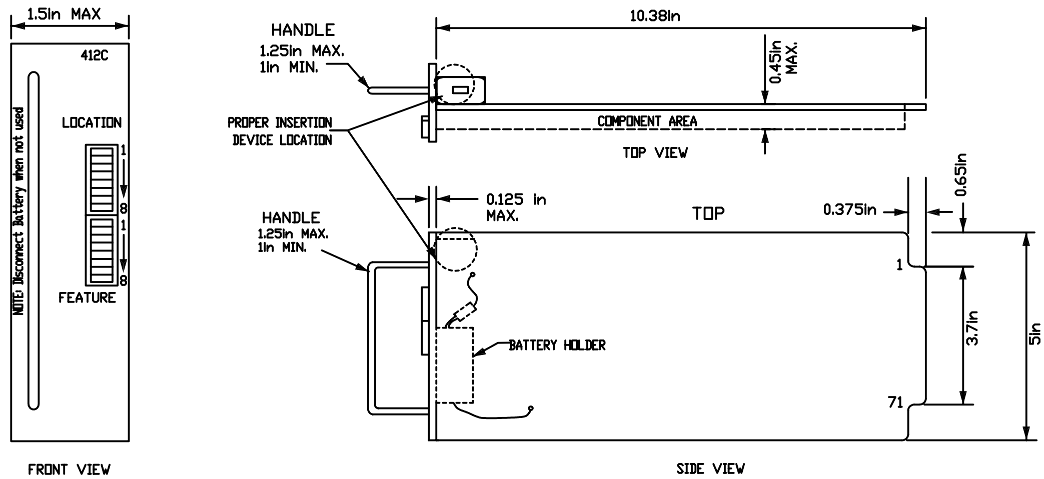
CONTACT	MODEL 400 FUNCTION
1	NA
2	AUDIO INPUT
3	AUDIO INPUT
4	NA
5	NA
6	NA
7	NA
8	NA
9	NA
10	NA
11	NA
12	NA
13	NA
14	NA
15	NA
16	NA
17	NA
18	NA
19	NA
20	NA
21	NA
22	NA

CIRCUIT SIDE

CONTACT	MODEL 400 FUNCTION
A	DC GROUND
B	DC GROUND
C	12 VDC
D	12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	CARRIER DETECT
L	REQUEST TO SEND
M	DATA INPUT
N	CLEAR TO SEND
P	DATA OUTPUT
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	AUDIO OUTPUT
Y	AUDIO OUTPUT
Z	NA

TITLE: MODEL 400 MODEM MODULE	
NO SCALE	A2-5
TEES 2008	

MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E



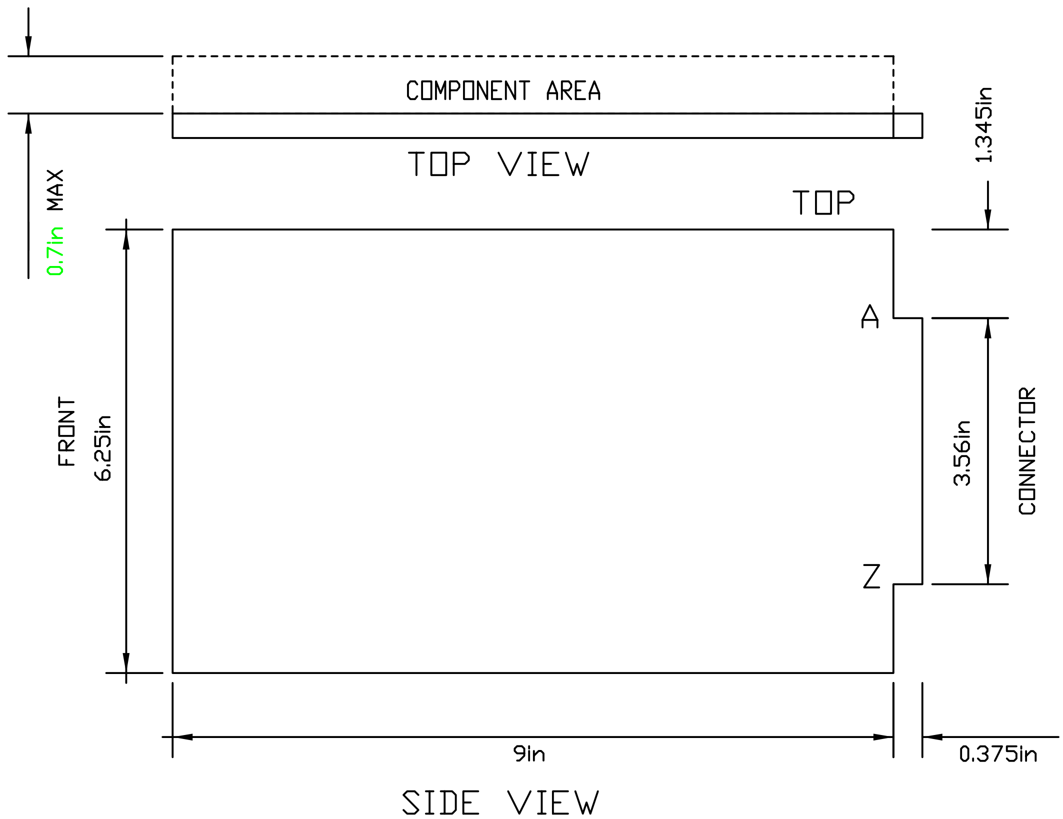
M170, M170E, AND 412C
PROGRAM MODULE CONNECTOR ASSIGNMENTS

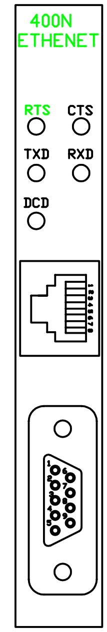
CIRCUIT SIDE		COMPONENT SIDE		M170 ONLY NOT REQUIRED BY 412C
FUNCTION	PCB CONNECTOR		FUNCTION	
A0	1	2	A1	
A2	3	4	A3	
A4	5	6	A5	
A6	7	8	A7	
A8	9	10	A9	
A10	11	12	A11	
A12	13	14	A13	
A14	15	16	A15	
$\overline{D0}$	17	18	$\overline{D1}$	
$\overline{D2}$	19	20	$\overline{D3}$	
$\overline{D4}$	21	22	$\overline{D5}$	
$\overline{D6}$	23	24	$\overline{D7}$	
$\overline{VMA}$ / Q2(E)	25	26	NA	RES
READ/WRITE	27	28	NA	NMI
NA	29	30	NA	ROT
NA	31	32	NA	
NA	33	34	EQUIP. GND	
NA	35	36	NA	RTS ACIA 4
NA	37	38	NA	CTS ACIA 4
NA	39	40	NA	DCD ACIA 4
NA	41	42	NA	TXD ACIA 4** (SEE NOTE)
NA	43	44	NA	RXD ACIA 4** (SEE NOTE)
NA	45	46	NA	
NA	47	48	NA	
NA	49	50	NA	
NA	51	52	NA	
NA	53	54	NA	
NA	55	56	NA	
NA	57	58	NA	
12 VDC	59	60	12 VDC	
-12 VDC	61	62	-12 VDC	
	KEY			
-5 VDC	63	64	-5 VDC	
5 VDC	65	66	5 VDC	
5 VDC	67	68	5 VDC	
GND	69	70	GND	
GND	*71	*72	GND	

* PINS 71 & 72 ON M170 & M170E CONNECTORS SHALL BE COMMONED. PINS 71 & 72 ON THE MODEL 412C SHALL BE TIED TO PINS 69 & 70.

** RELATIVE TO THE ACIA

TITLE: MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E	
NO SCALE	A2-6
TEES 2008	



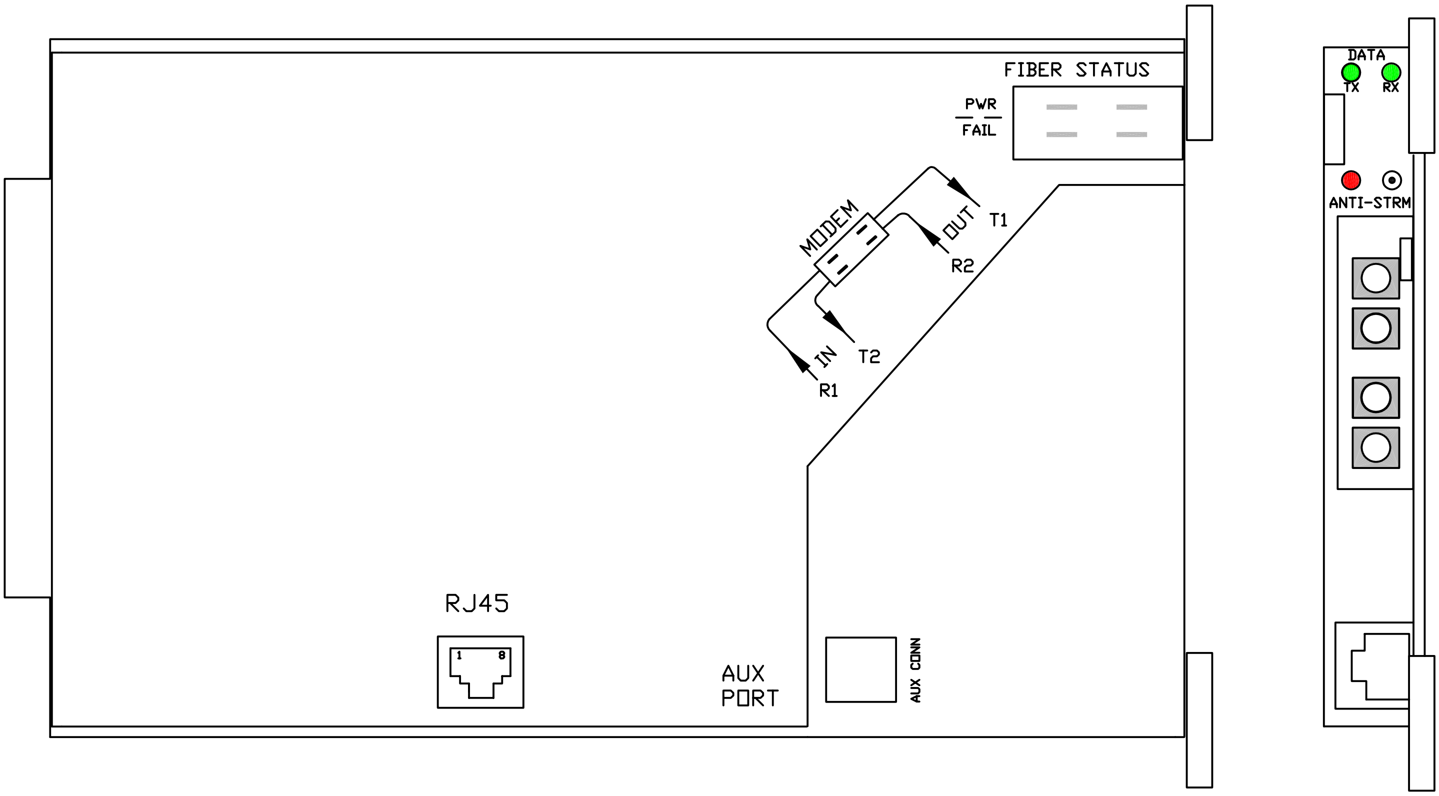


CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA

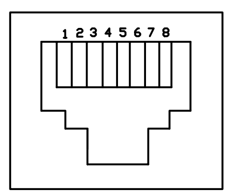
DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	DC GND
6	NA
7	RTS
8	CTS
9	NA

RJ45 ETHERNET PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	NA
3	RX +	7	NA
4	RX-	8	NA

TITLE: MODEL 400N ETHERNET MODULE	
NO SCALE	A2-7
TEES 2008	



CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA



RJ45 (detail)

RJ45 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	NA	5	RXD
2	CD	6	TXD
3	NA	7	CTS
4	GND	8	RTS

TITLE:

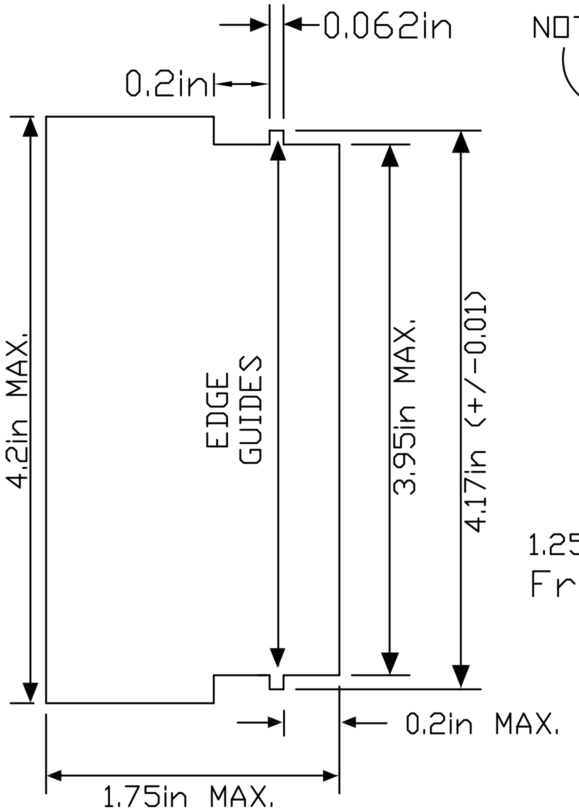
MODEL 400F FIBER MODULE

NO SCALE

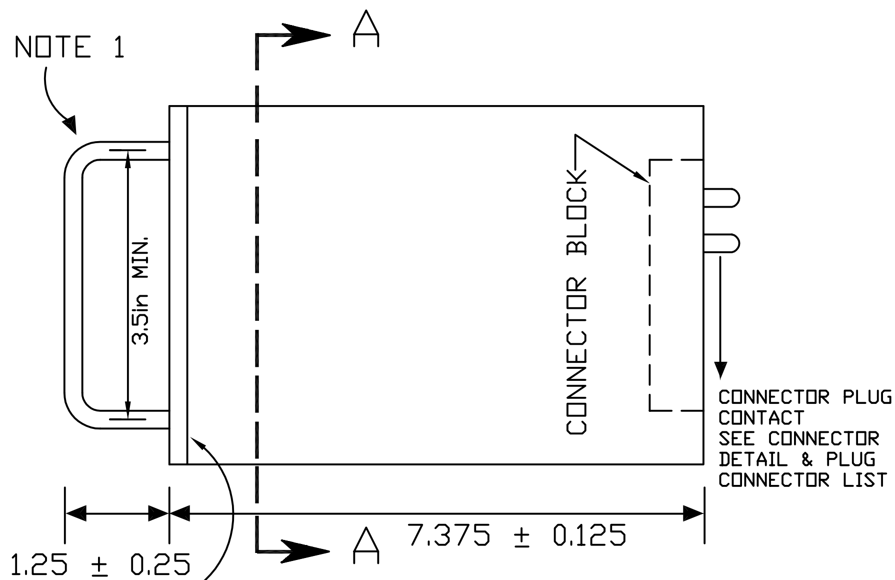
TEES 2008

A2-8

APPENDIX A3
CHAPTER 3 DETAILS



CROSS SECTION A-A



SIDE VIEW

MODEL PLUG CONNECTORS LIST
(OR EQUAL)

MODEL 200 - BEAU P-5412-LAB
MODEL 204 - BEAU P-5406-LAB
MODEL 205 - BEAU P-5408-LAB

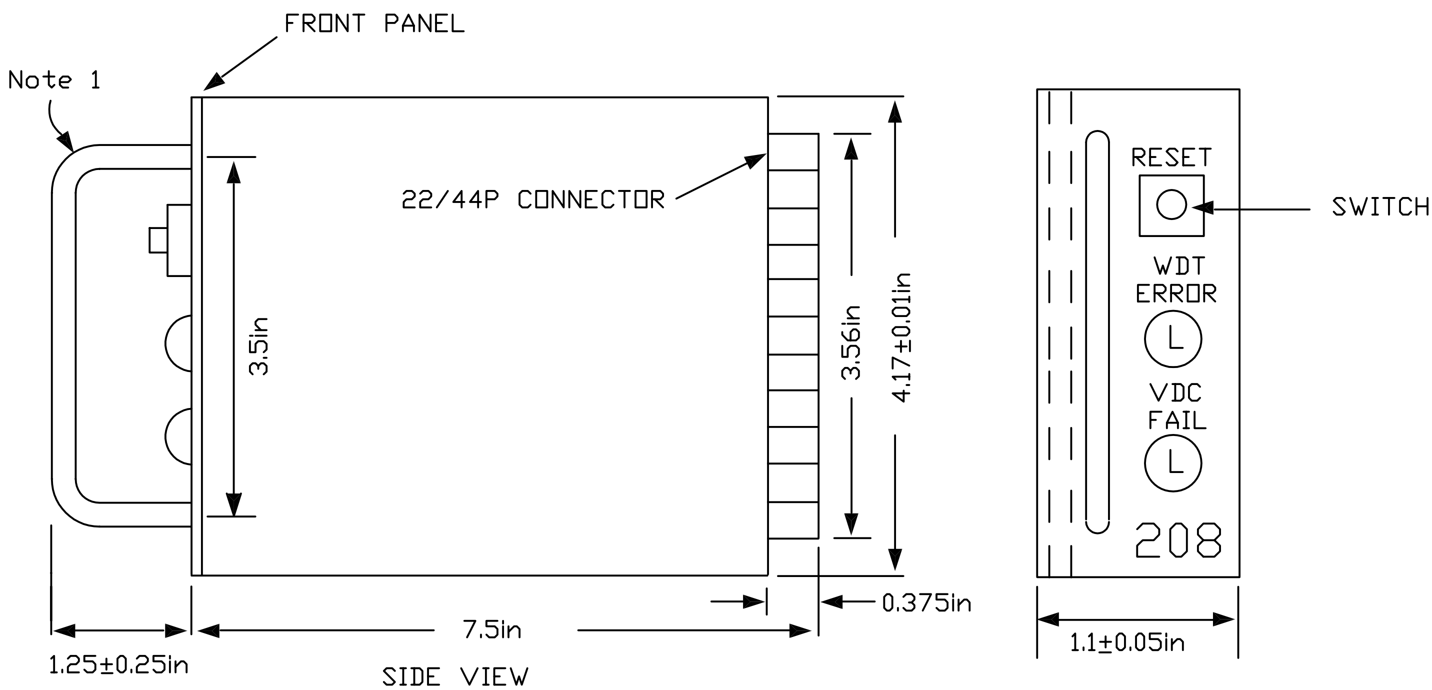
MODEL 200, 204 & 205 CONNECTOR DETAIL

PIN	FUNCTION	PIN	FUNCTION	PIN	Function
1	AC+	7	Load Circuit #1	1	Coil
2	Equip. Ground	8	Load Circuit #2	2	Coil
3	Red Output	9	Equip. Ground	3	NC CKT1
4	Not Assigned	10	AC-	4	NC CKT2
5	Yellow Output	11	AC+	5	Common CKT1
6	Red Input	12	Not Assigned	6	Common CKT2
7	Green Output			7	NO CKT1
8	Yellow Input			8	NO CKT2
9	+24 VDC				
10	Green Input				
11	AC-				
12	Not Assigned				

NOTE:

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter stock to form a handle.

TITLE: MODEL 200 SWITCH PACK, 204 & 205 CONNECTOR DETALS	
NO SCALE	A3-1
TEES 2008	



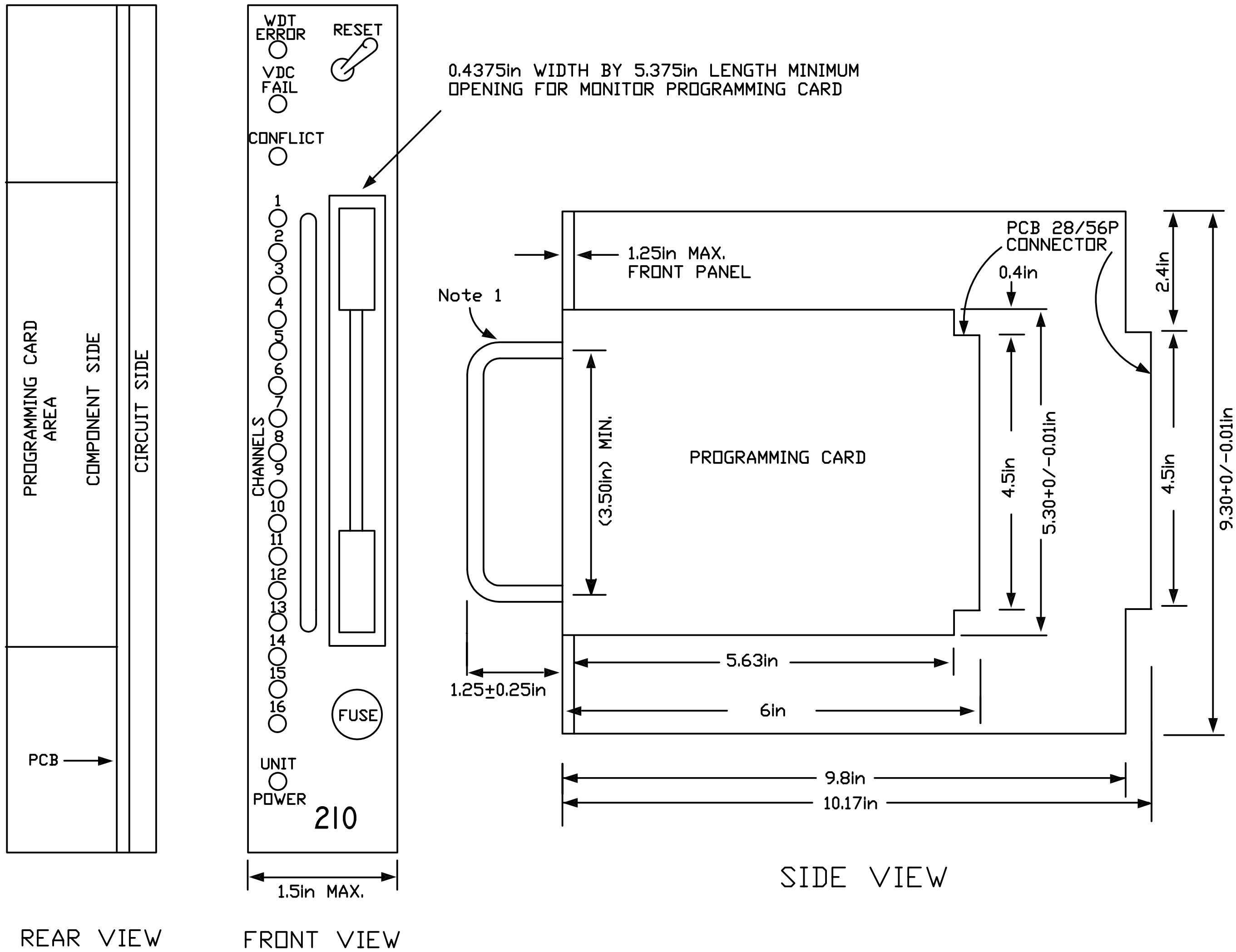
MODEL 208 MONITOR UNIT PIN ASSIGNMENT

PIN	FUNCTION
1/A	DC Ground
2/B	WDT Ext. Reset
5/E	WDT IN
10/L	+24 VDC
15/S	AC-
17/U	Normally Open, Circ. #2
19/W	AC+
20/X	WDT Lamp (External)
21/Y	Circ. Common #1 & #2
22/Z	Normally Closed, Circ. #1

NOTE:

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter stock to form a handle.

TITLE: MODEL 208 T170 MONITOR UNITS	
NO SCALE	A3-2
TEES 2008	



NOTE (for A3-3 & A3-4):

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter stock to form a handle.

2. Model 210 tolerance dimensions are +/- 0.02 in except as noted.

3. Sheet definitions:
   ---= Slotted for keying.
   (C) = Collector
   (E) = Emitter
   * = NA for these connections on models 232 & 242.

TITLE: MODEL 210 T170 MONITOR UNIT	
NO SCALE	A3-3
TEES 2008	

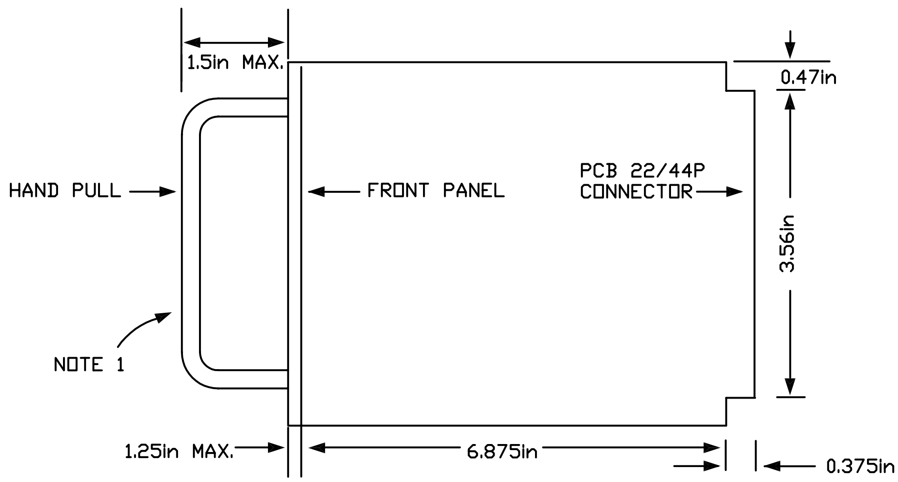
MODEL 210 MONITOR UNIT CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION	Pin	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #6 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #8 Yellow	F	Channel #16 Green
7	Channel #5 Green	H	Channel #5 Green
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 Green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC− *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25	BB	Stop Time
25	Tied Together)	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

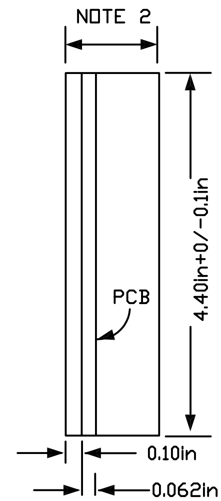
MODEL 210 PROGRAMMING CARD CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION (Circuit Side)	Pin	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #15 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

TITLE: MODEL 210 T170 MONITOR UNIT PROGRAMMING CARD CONNECTOR & WIRING ASSIGNMENTS	
NO SCALE	A3-4
TEES 2008	



SIDE VIEW



END VIEW

MODEL 222, 224, & 232
CONNECTOR ASSIGNMENTS

PIN	FUNCTION
A	DC Ground
B	+24 VDC
- - -	
*C	Detector Reset
D	# 1 Input
E	# 1 Input
F	# 1 Output (C)
H	# 1 Output (E)
J	# 2 Input
K	# 2 Input
L	Equipment Ground
M	AC-
- - -	
N	AC+
P	# 3 Input
R	# 3 Input
S	# 3 Output (C)
T	# 3 Output (E)
U	# 4 Input
V	# 4 Input
W	# 2 Output (C)
X	# 2 Output (E)
Y	# 4 Output (C)
Z	# 4 Output (E)

MODEL 242 & 252
CONNECTOR ASSIGNMENTS

PIN	FUNCTION
*A	DC Ground
*B	+24 VDC
- - -	
C	NA
D	# 1 Input
E	# 1 Input Common
F	# 1 Output (C)
H	# 1 Output (E)
J	# 2 Input
K	# 2 Input Common
L	Equipment Ground
M	AC-
- - -	
N	AC+
P	NA
R	NA
S	NA
T	NA
U	NA
V	NA
W	# 2 Output (C)
X	# 2 Output (E)
Y	NA
Z	NA

NOTE:

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter stock to form a handle.

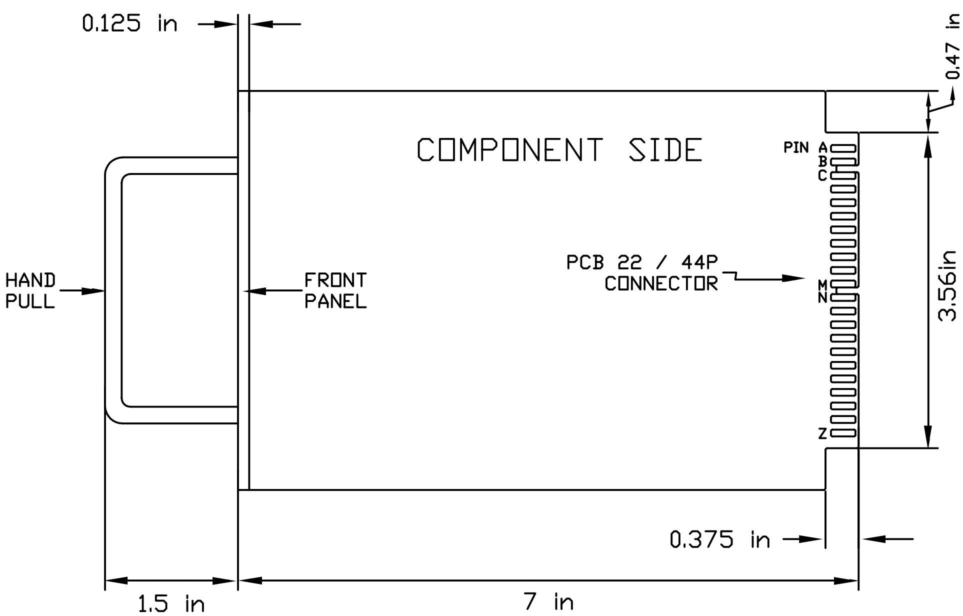
2. Models 222, 232, 242 and 252 shall have a width of 1.12in. Model 224 shall have a width of 2.0+/-0.25.

3. Sheet definitions:
   - - - = Slotted for keying.
   (C) = Collector
   (E) = Emitter
   * = NA for these connections on models 232 & 242.

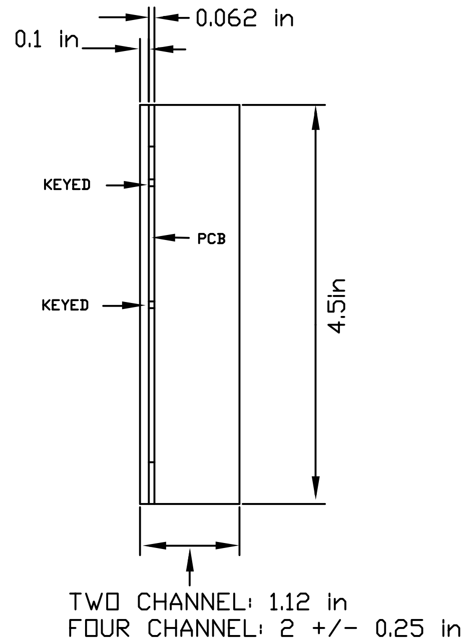
TITLE: MODELS 222, 224, 232, 242 AND 252	
NO SCALE	A3-5
TEES 2008	

APPENDIX A4
CHAPTER 4 DETAILS

APPENDIX A5
CHAPTER 5 DETAILS



SIDE VIEW



END VIEW

CONNECTOR ASSIGNMENTS

PIN	ISOLATORS	SENSORS
A	DC GROUND	
B	+24 VDC	
C	N/A	EXT RESET
D	INPUT #1	
E	INPUT #1	
F	OUTPUT #1 (C)	
H	OUTPUT #1 (E)	
J	INPUT #2	
K	INPUT #2	
L	EQUIPMENT GROUND	
M	AC-	
N	AC+	
P	N/A	INPUT #3
R	N/A	INPUT #3
S	N/A	OUTPUT #3 (C)
T	N/A	OUTPUT #3 (E)
U	N/A	INPUT #4
V	N/A	INPUT #4
W	OUTPUT #2 (C)	
X	OUTPUT #2 (E)	
Y	N/A	OUTPUT #4 (C)
Z	N/A	OUTPUT #4 (E)

NOTES:

1. TOLERANCE DIMENSIONS ARE +/-0.02 in EXCEPT AS NOTED.
2. "U" SHAPE ROD HANDLE SHALL BE FABRICATED OF 0.18 in TO 0.26 in DIAMETER STOCK.

TITLE: SENSOR UNIT AND ISOLATOR DETAILS

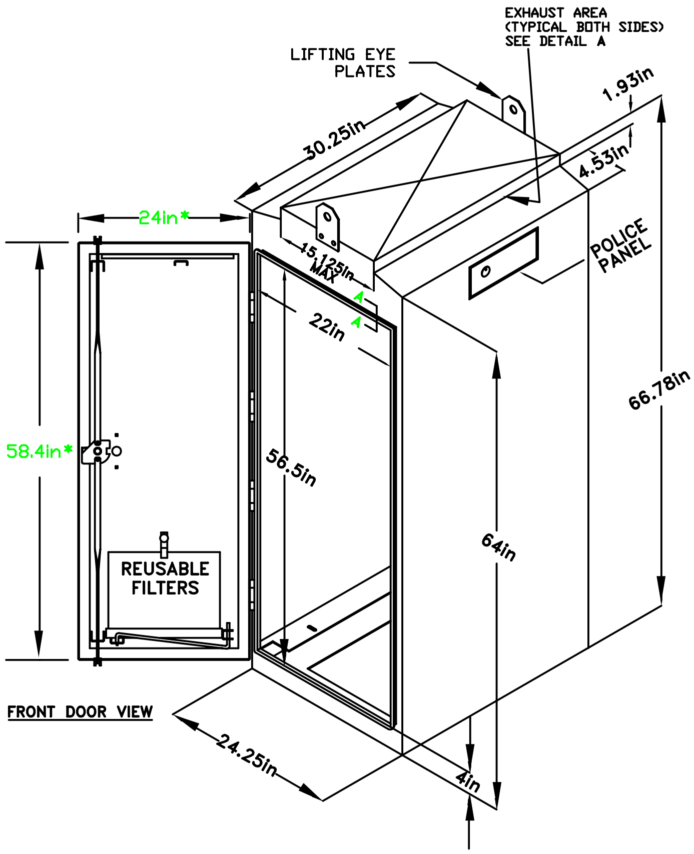
NO SCALE

TEES 2008

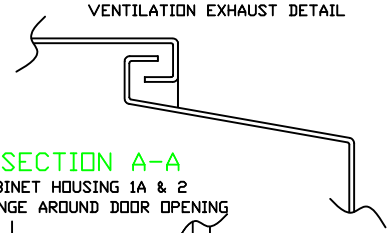
A5-1

APPENDIX A6
CHAPTER 6 DETAILS

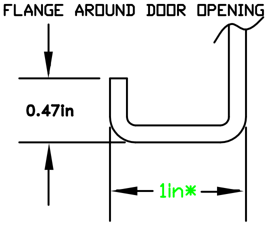
CABINET HOUSING 1B



DETAIL A
CABINET HOUSING 1B & 2
VENTILATION EXHAUST DETAIL



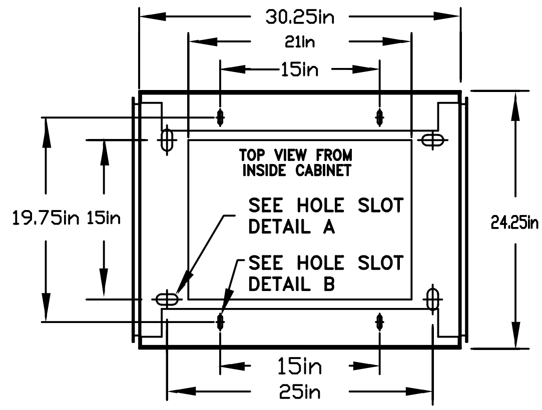
SECTION A-A
CABINET HOUSING 1A & 2
FLANGE AROUND DOOR OPENING



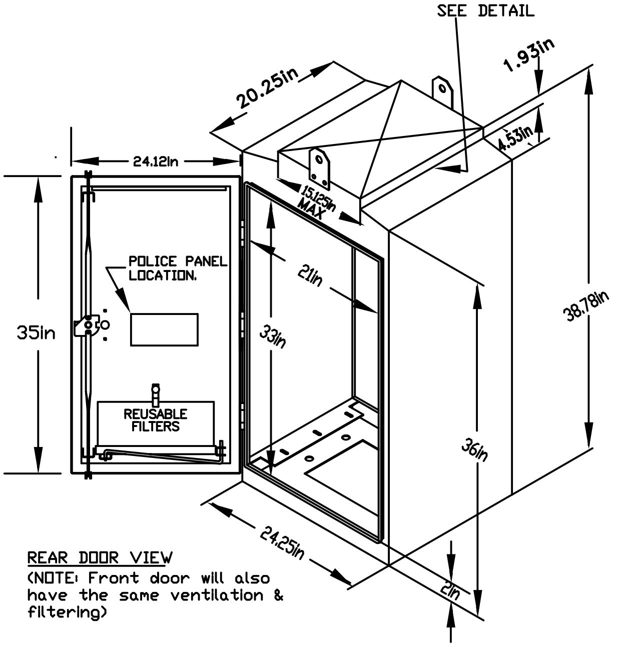
* TOLERANCE +0.0625, -0

NOTE: ALL HOLE PATTERNS CENTERED ON CABINET BOTTOMS.

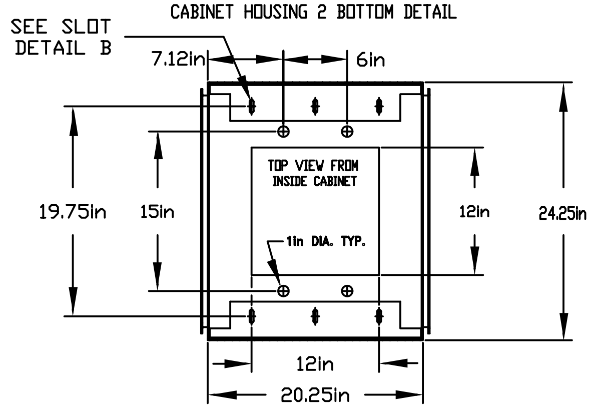
CABINET HOUSING 1B BOTTOM DETAIL



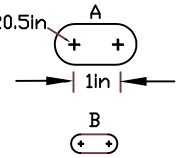
CABINET HOUSING 2



CABINET HOUSING 2 BOTTOM DETAIL



Hole slot detail



0.375inx1.25in OBROUND

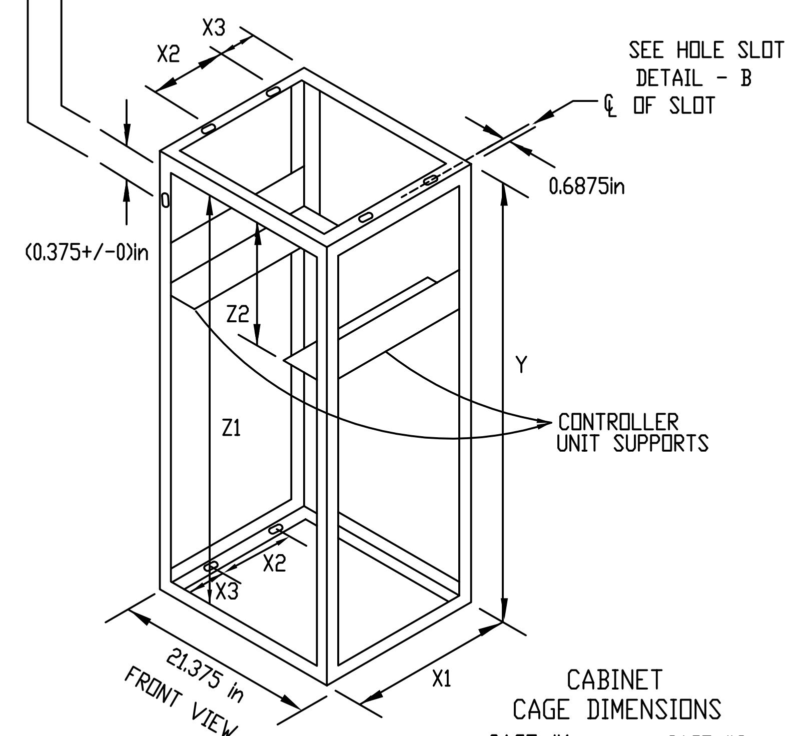
TITLE: CABINET HOUSING DETAILS
SHEET 1 OF 4

NO SCALE

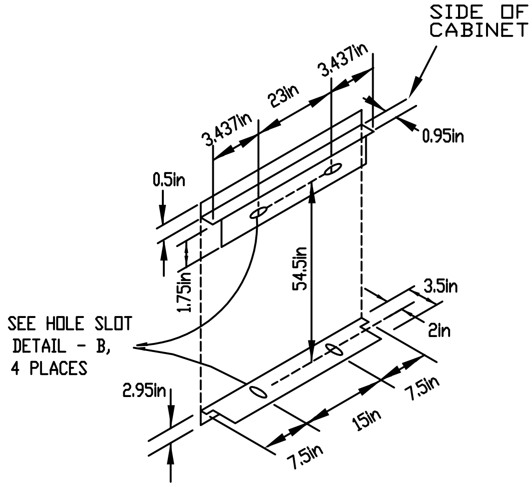
TEES 2008

A6-1

CAGE SUPPORT DETAIL



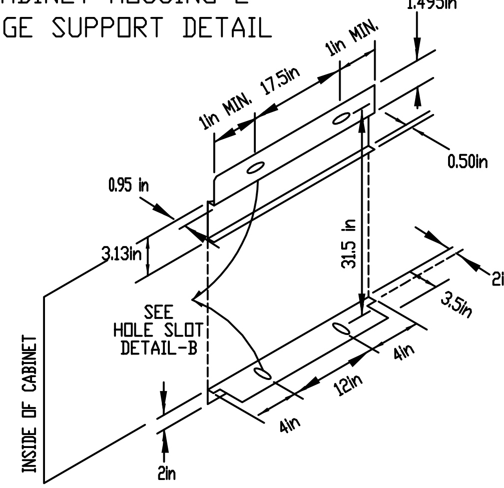
CABINET HOUSING 1B CAGE SUPPORT DETAIL



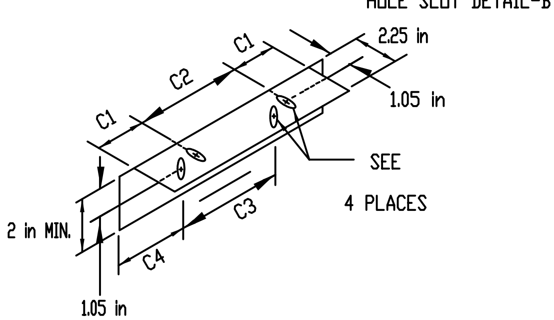
CABINET CAGE DIMENSIONS

	CAGE #1	CAGE #2
X1	21.38in	16in
X2	15in	12in
X3	3.188in	2in
Y	55.5in	32.5in
Z1	53in MIN.	31in MIN.
Z2	15.75in	7.25in

CABINET HOUSING 2 CAGE SUPPORT DETAIL

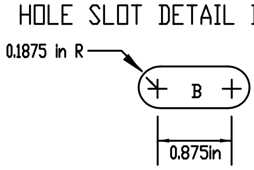


SPACER BRACKET DETAIL



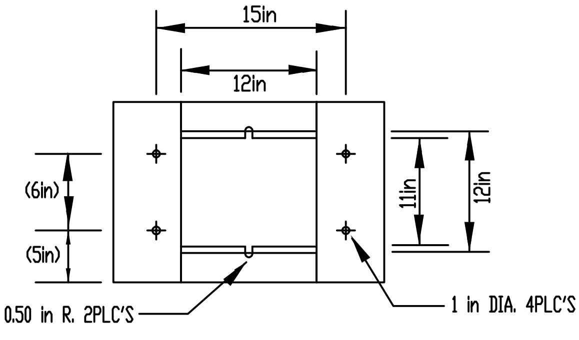
	CAGE #1	CAGE #2
C1	3 in MIN.	3 in MIN.
C2	15in	12 in
C3	23 in	17.5 in
C4	1 in MIN.	1 in MIN..

HOLE SLOT DETAIL B



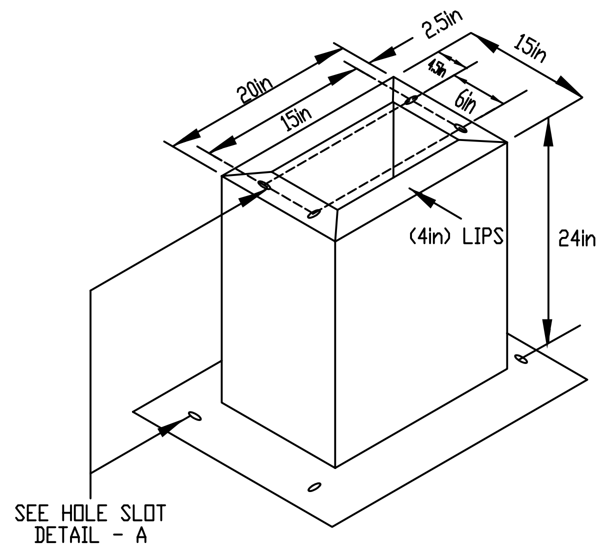
TITLE: CABINET HOUSING DETAILS SHEET 2 OF 4	
NO SCALE	A6-2
TEES 2008	

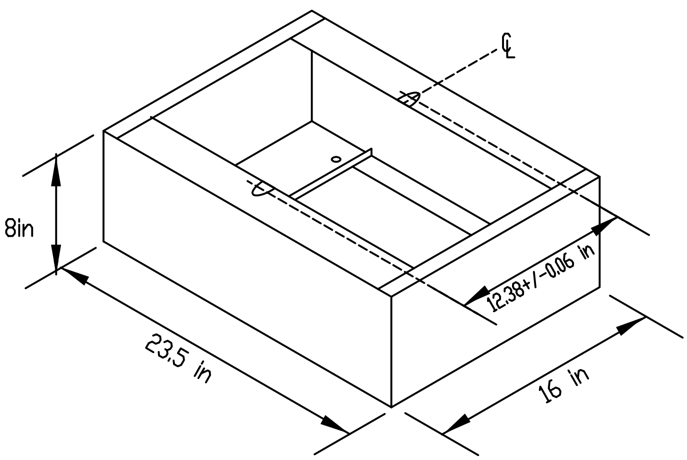
CABINET HOUSING 2
"M" BASE ADAPTOR DETAIL



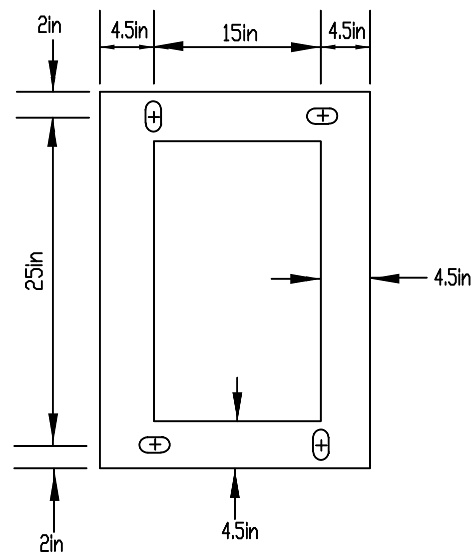
TOP VIEW

TYPE 332/336 ADAPTOR



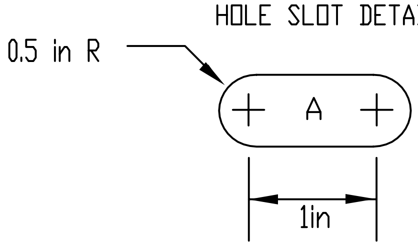


BOTTOM VIEW



332 BASE VIEW

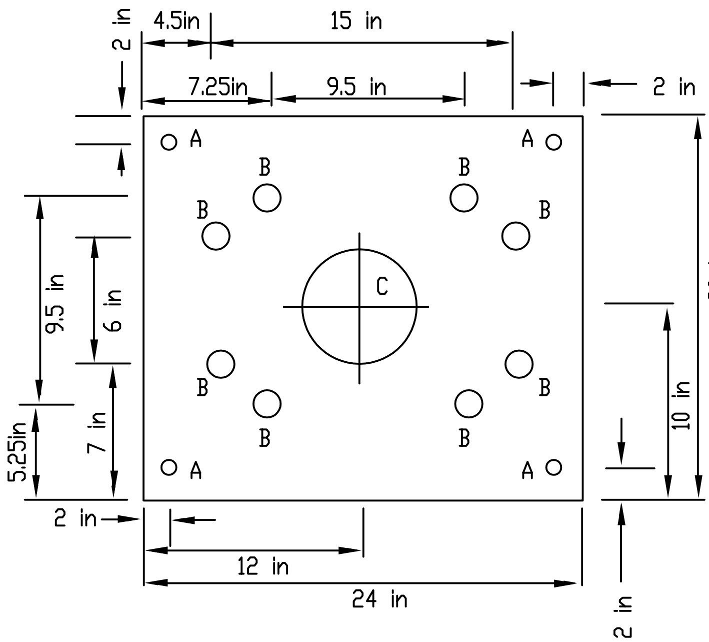
HOLE SLOT DETAIL



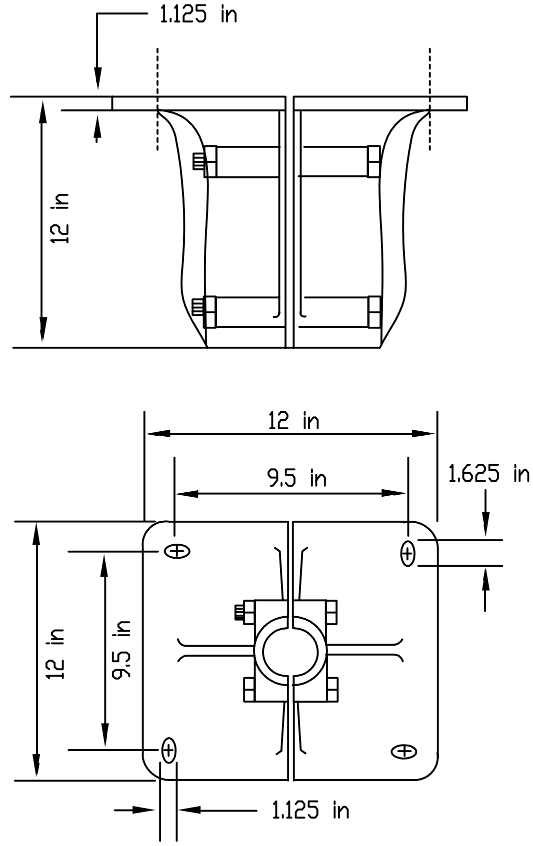
DETAIL - A

TITLE: CABINET HOUSING DETAILS SHEET 3 OF 4	
NO SCALE	A6-3
TEES 2008	

CABINET HOUSING 2
PEDESTAL ADAPTOR

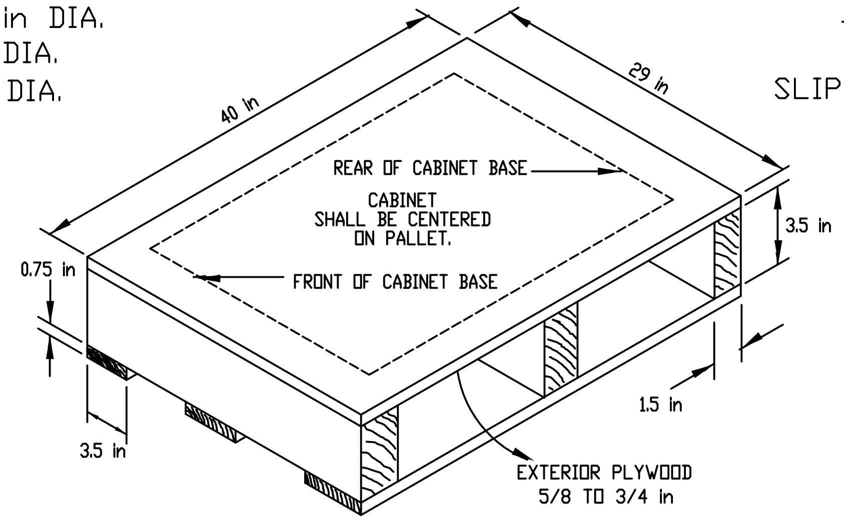


SLIPFITTER BASE PLATE
DETAIL
(0.375 in ALUMINUM)



SLIPFITTER (CAST ALUMINUM)
DETAIL

A = 0.50 in DIA.
B = 1 in DIA.
C = 5 in DIA.



CABINET PALLET

<u>NOTE:</u> (for details A6-1 to A6-4)

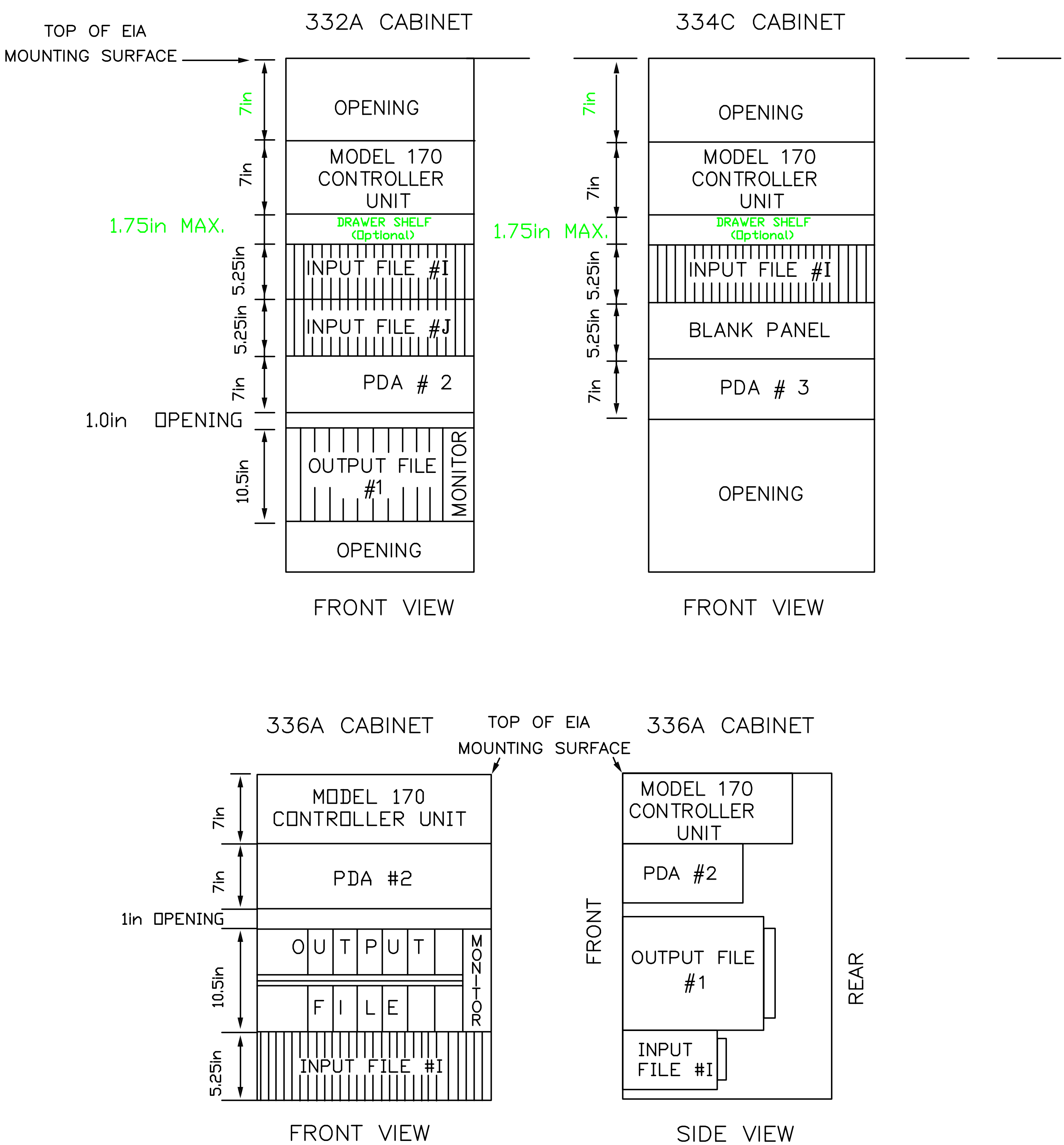
1. Housing 1B used in cabinets 332 & 334 and Housing 2 in cabinet 336.
2. Adaptors delivered separately shall be delivered centered and bolted on a plyboard shipping pallet.
3. Dashed lines on cabinet cage support detail delineates the cabinet side wall.
4. The bottom cabinet cage supports shall be continuously welded along the sides of the cabinet & extended to the inside corner of door openings.
   The top cabinet cage supports shall be continuously welded along the sides of the cabinet.
5. Cage support hole slots dimension shall be common for top & bottom.

TITLE: CABINET HOUSING DETAILS
SHEET 4 OF 4

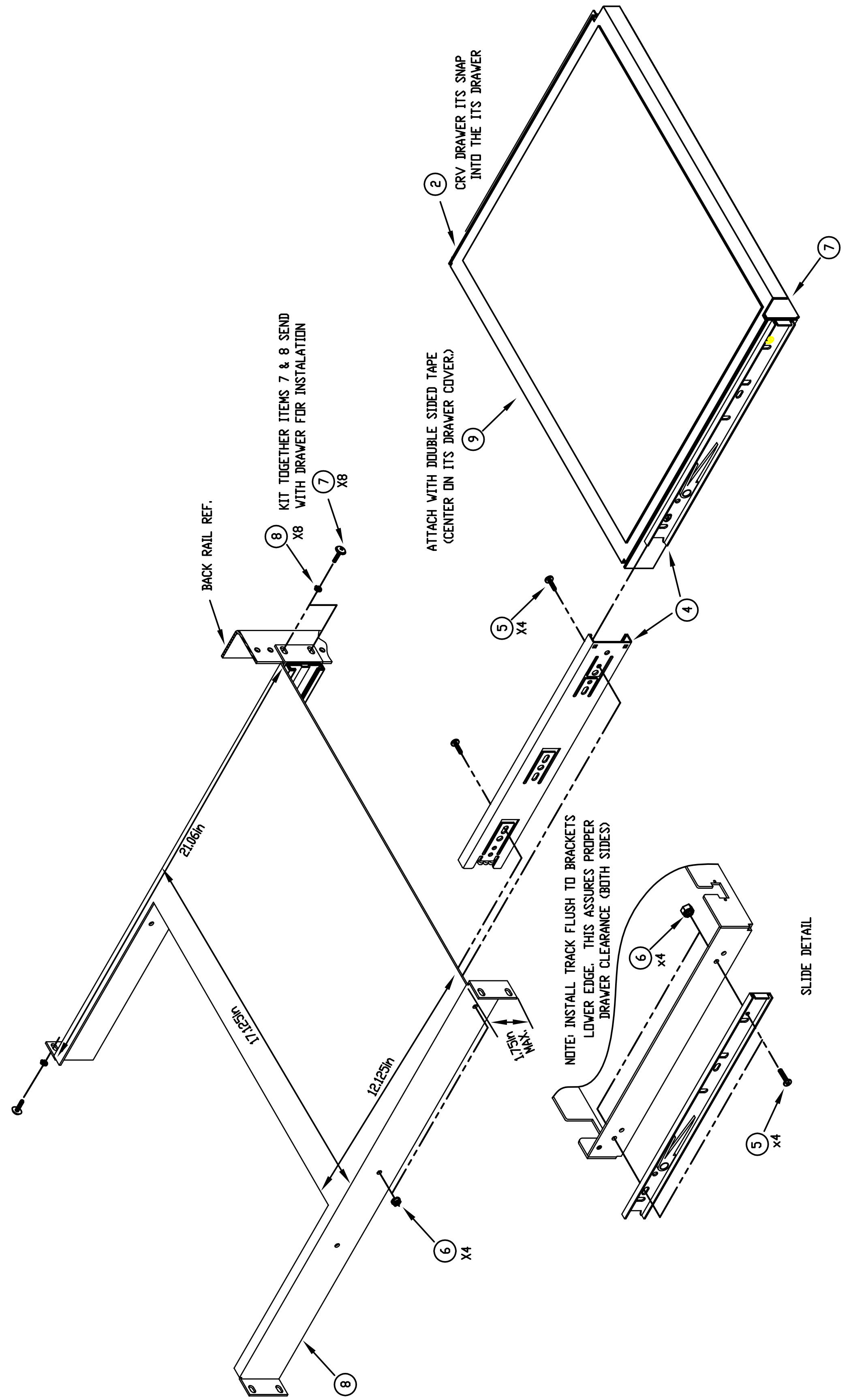
NO SCALE

TEES 2008

A6-4



TITLE: CABINET EQUIPMENT MOUNTING DETAIL SHEET 1 OF 5	
NO SCALE	A6-5
TEES 2008	



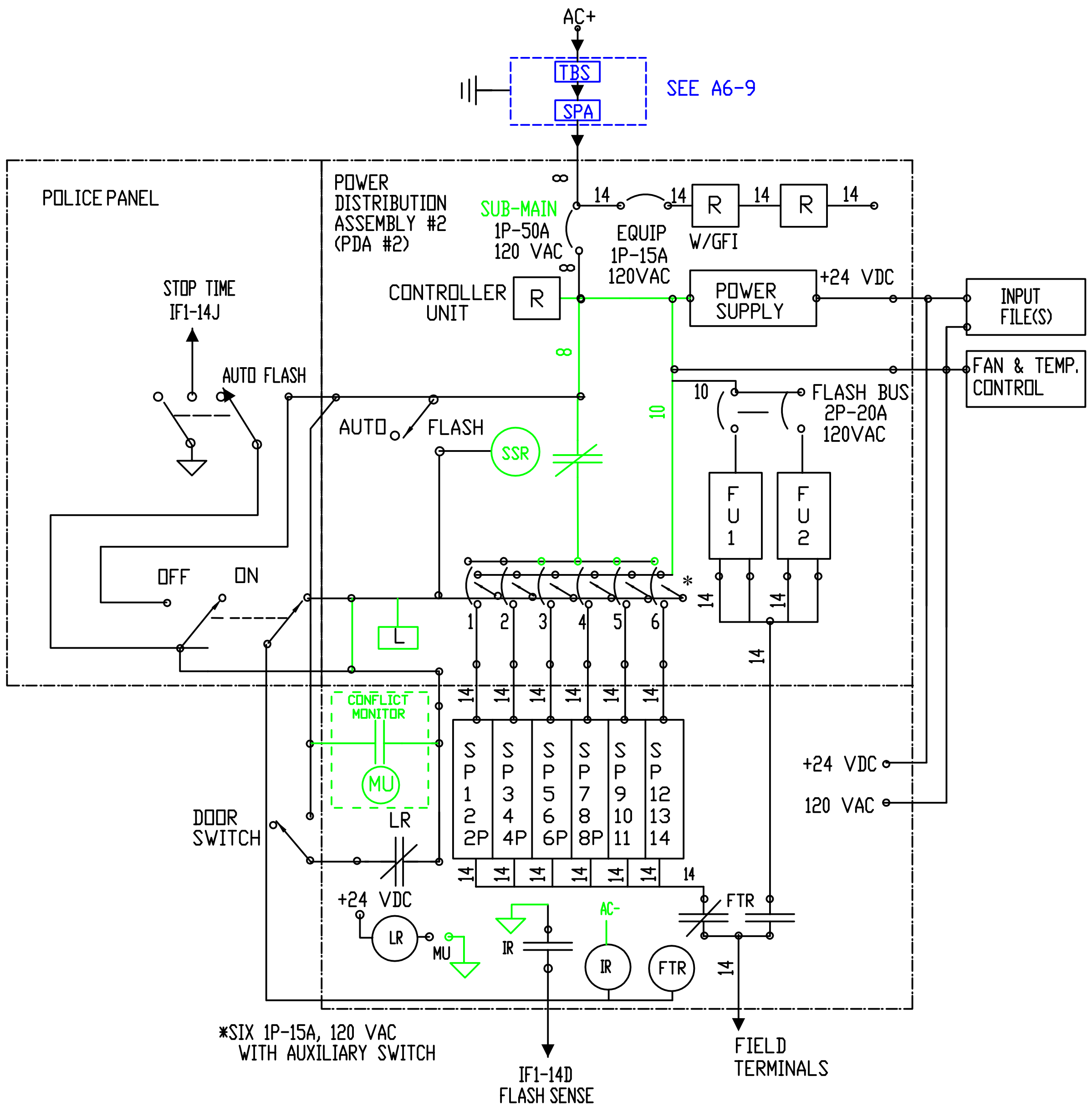
TITLE:

DRAWER SHELF UNIT

SHEET 2 OF 5

NO SCALE	A6-6
TEES 2008	

332A & 336 CABINET
ONE LINE DIAGRAM



SHEET DEFINITIONS

TBS	TERMINAL BLOCK - SERVICE		RELAY COIL - * RELAY NAME	TR	TRANSFER RELAY
	EQUIPMENT GROUND	FU1	FLASHER UNIT ONE	IR	ISOLATION RELAY
8	WIRE SIZE, IF NOT INDICATED SHALL BE #16 AWG OR LARGER		DC GROUND		SWITCH CONTACT
		WDT	WATCHDOG TIMER	LR	LOGIC RELAY
	CIRCUIT BREAKER	FTR	FLASH TRANSFER RELAY	CB-1	SIGNAL CIRCUIT BREAKER 1 (SECONDARY)
R	DUPLEX RECEPTACLE	L	PDA FLASH ON DISPLAY LAMP	IF-14U	INPUT FILE 1, TERM. BLOCK 14, POSITION U
WGFI	WITH GROUND FAULT INTERRUPTER	MU	MONITOR UNIT	T2-6	TERMINAL BLOCK 2, POSITION 6
	RELAY CONTACT, NORMALLY CLOSED	SPA	SERVICE PANEL ASSEMBLY	C1-65	C1 CONNECTOR, PIN 65
	RELAY CONTACT, NORMALLY OPEN				
SSR	SOLID STATE RELAY				

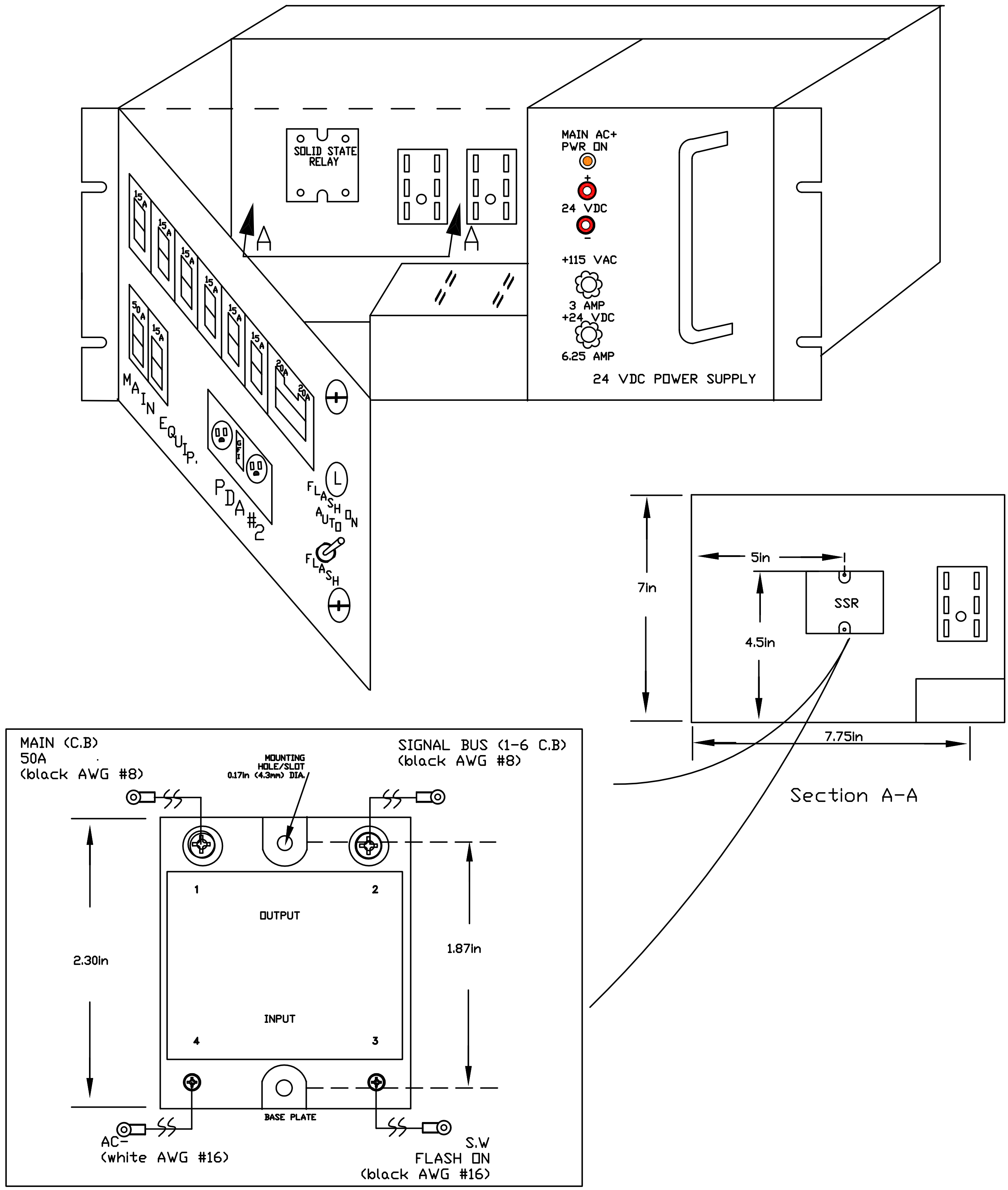
TITLE: CABINET EQUIPMENT MOUNTING DETAIL

SHEET 3 OF 5

NO SCALE

TEES 2008

A6-7



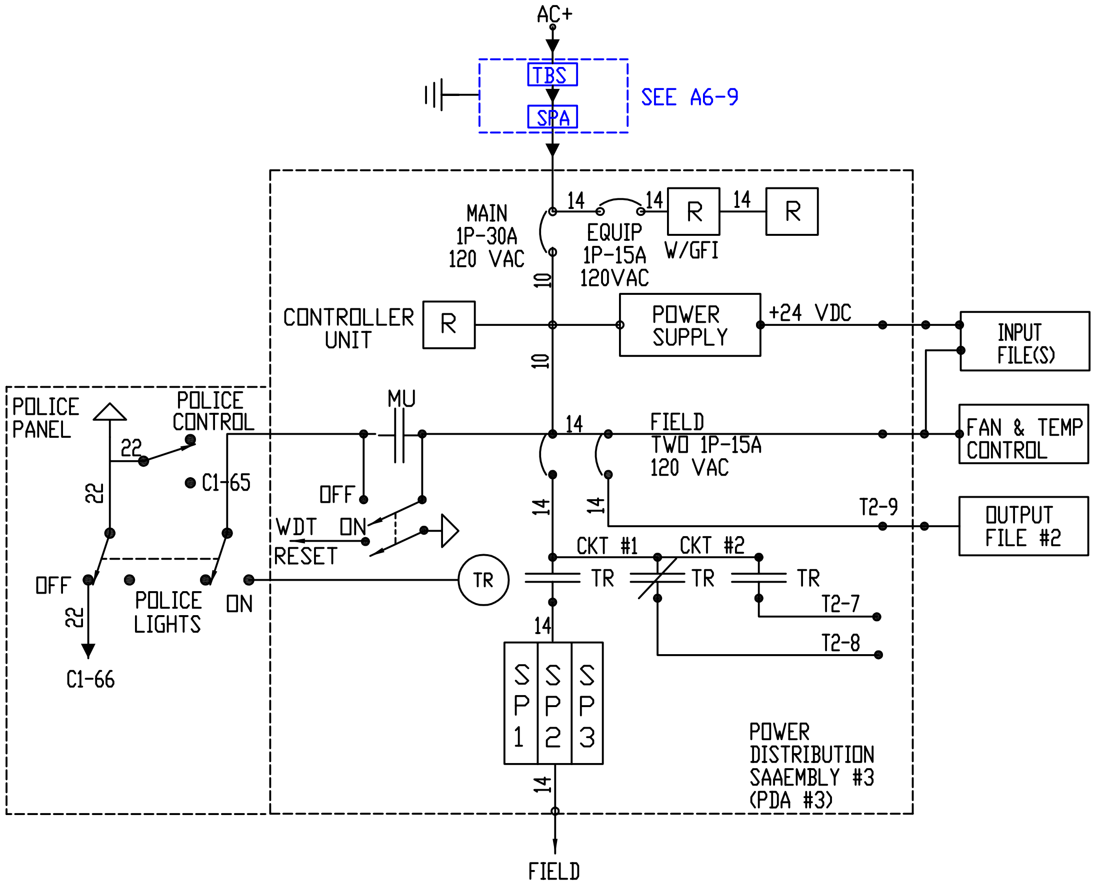
TITLE:

SOLID STATE RELAY DETAILS

SHEET 4 OF 5

NO SCALE	A6-8
TEES 2008	

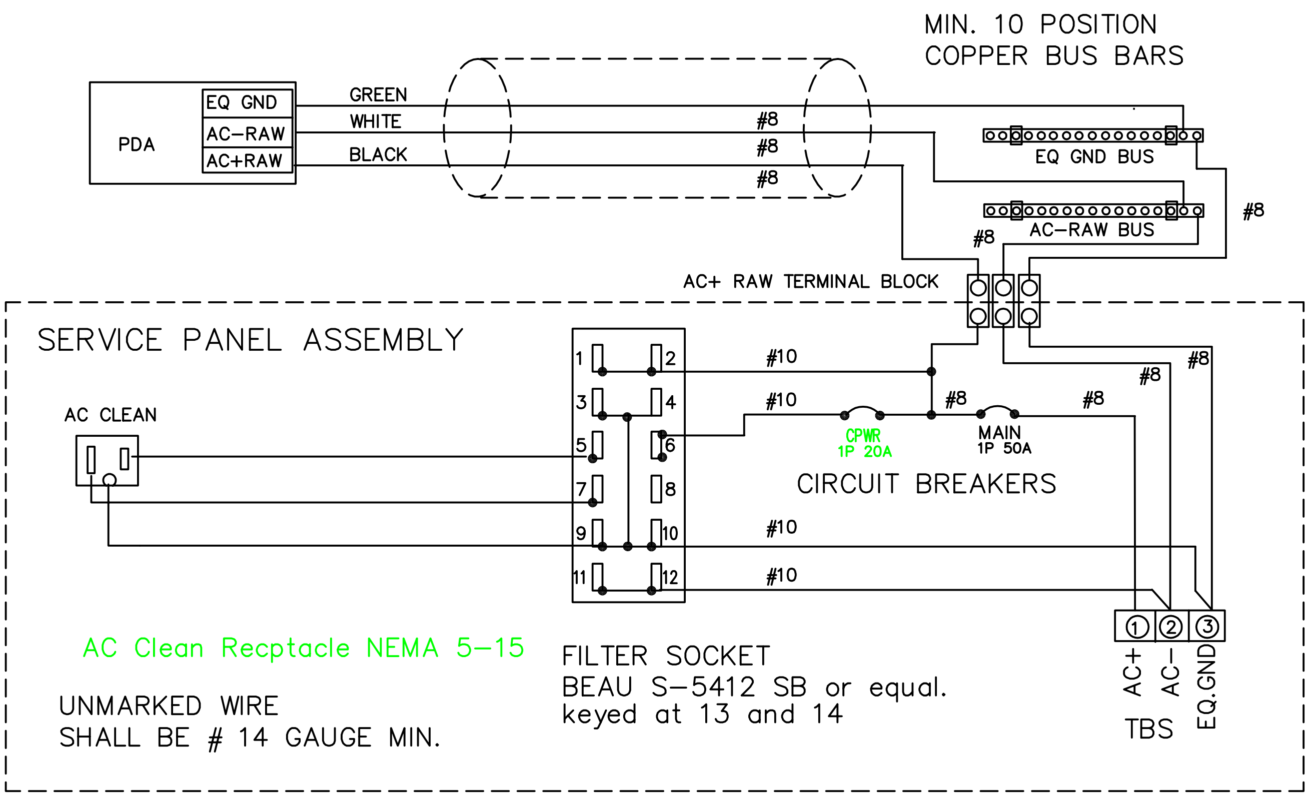
334C CABINET ONE LINE DIAGRAM



SHEET DEFINITIONS

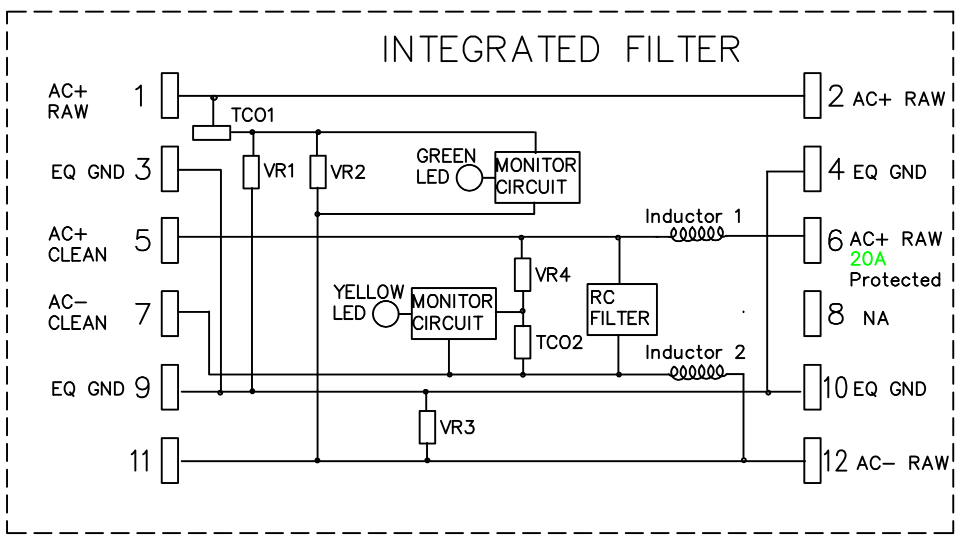
TBS	TERMINAL BLOCK - SERVICE	WDT	WATCHDOG TIMER
	EQUIPMENT GROUND	MU	MONITOR UNIT
8	WIRE SIZE, IF NOT INDICATED SHALL BE #16 AWG OR LARGER	CB-1	SIGNAL CIRCUIT BREAKER 1 (SECONDARY)
	CIRCUIT BREAKER	TR	TRANSFER RELAY
R	DUPLEX RECEPTACLE	T2-6	TERMINAL BLOCK 2, POSITION 6
WGFI	WITH GROUND FALUT INTERRUPTER	C1-65	C1 CONNECTOR, PIN 65
	RELAY CONTACT, NORMALLY CLOSED	IF-14D(J)	INPUT FILE 1, TERM BLOCK 14, POSITION D OR J
	RELAY CONTACT, NORMALLY OPEN		DC GROUND
SPA	SERVICE PANEL ASSEMBLY		
	FLASHER UNIT ONE		SWITCH CONTACT

TITLE: CABINET EQUIPMENT MOUNTING DETAIL SHEET 5 OF 5	
NO SCALE	A6-9
TEES 2008	

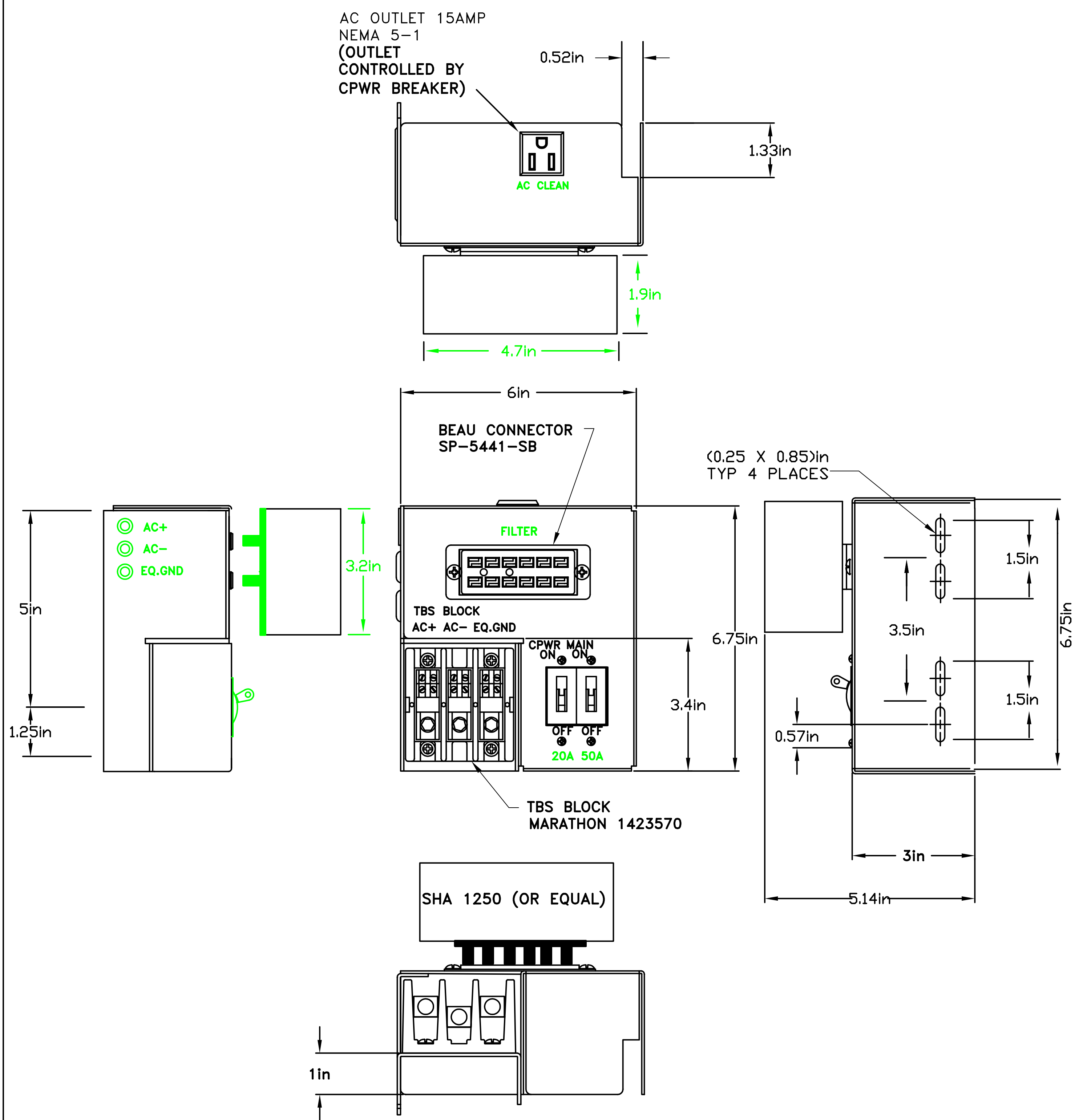


Notes: (for details A6-10 & A6-11)

1. VR1,2 and 4 are 100 joule Movistors rated with 200V clamping
2. VR3 is 135 joule rated Movistors with 250V clamping
3. TC/TF01 and 2 Thermal Cut Off/Fuse Protection for the Movistors
4. Inductor 1 and 2 rated 30 MicroHenries at 20A
5. RC filter system 10 DB at 10 KHZ, 50 DB at 100 KHZ and 90 DB at 1 Mhz.
6. GREEN LED Indicator ON= ok, OFF= error.
7. YELLOW LED ON= error, Off= ok
8. CPWR: Clean Power
9. TBS: Termial Block Service



TITLE: SERVICE PANEL ASSEMBLY SCHEMATIC SHEET 1 OF 2	
NO SCALE	A6-10
TEES 2008	



TITLE: SERVICE PANEL ASSEMBLY

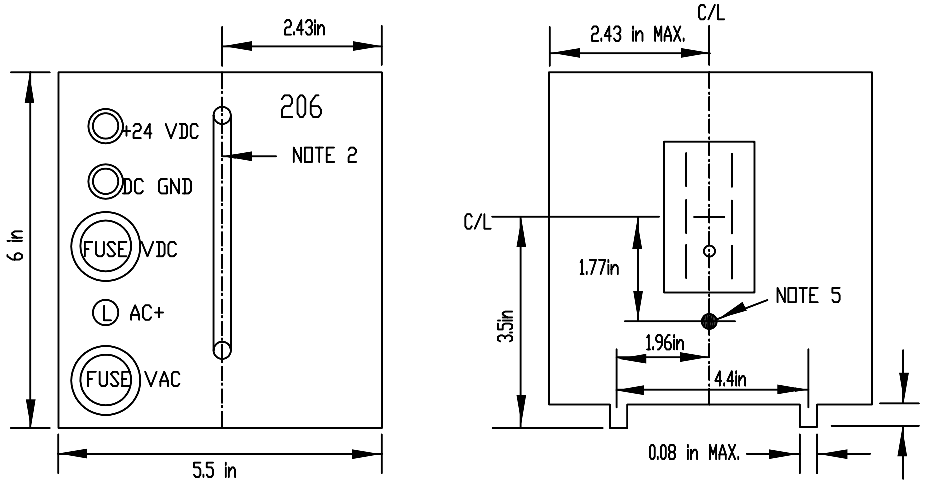
SHEET 2 OF 2

NO SCALE

TEES 2008

A6-11

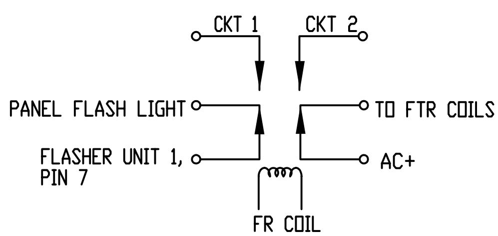
MODEL 206 POWER SUPPY MODULE



FRONT VIEW

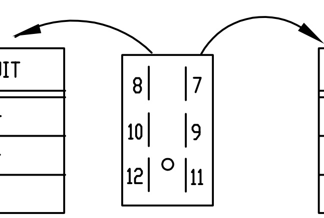
REAR VIEW

FLASH RELAY CONNECTOR SOCKET WIRING DETAIL



FLASHER UNIT CONNECTOR SOCKET WIRING DETAIL

PIN NO.	CIRCUIT	PIN NO.	CIRCUIT
7	LD Ckt #1	10	AC-
8	LD Ckt #2	11	AC+
9	EG	12	NA



(REAR VIEW)

POWER SUPPLY MODULE WIRING DETAIL

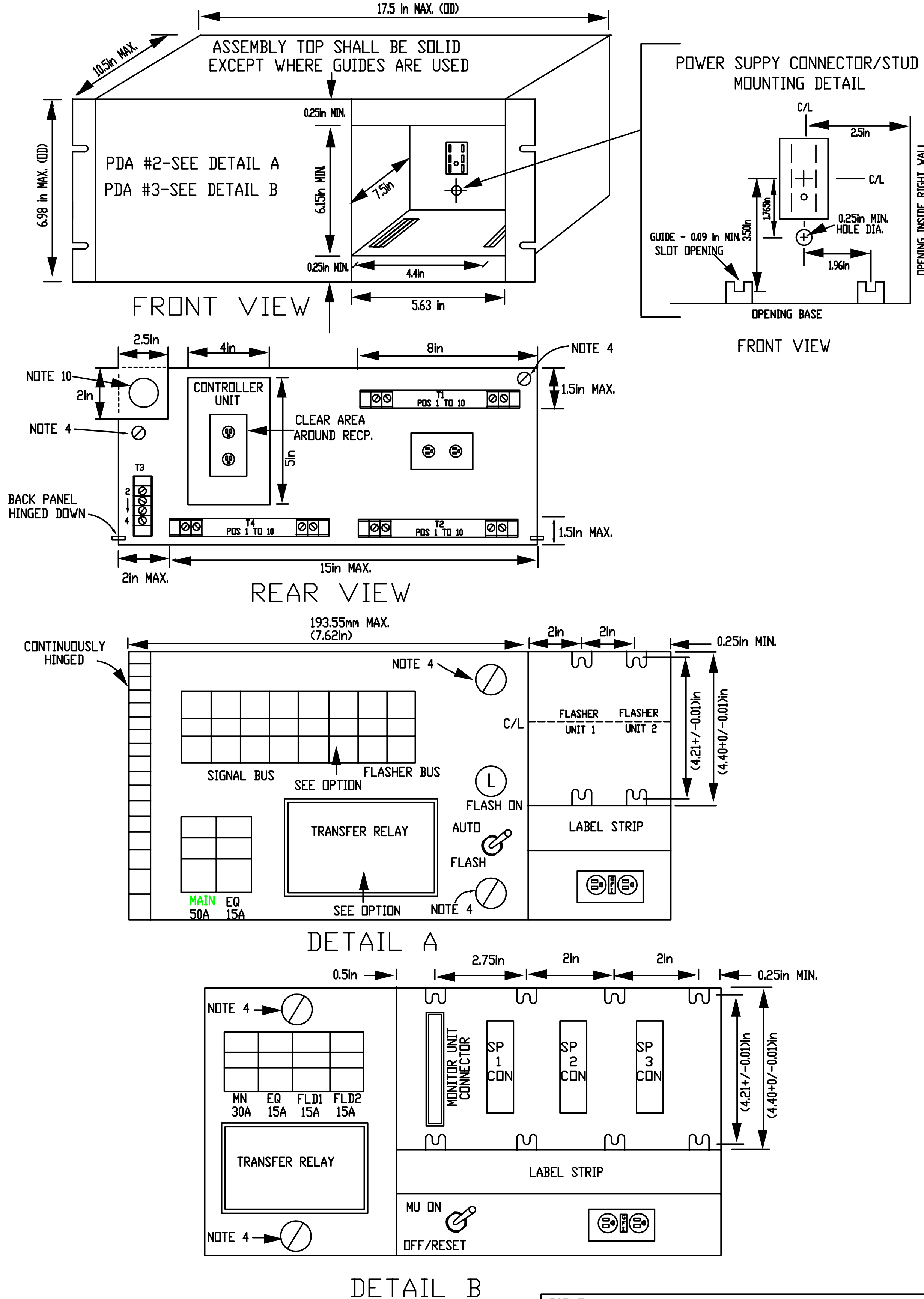
PIN NO.	CIRCUIT	PIN NO.	CIRCUIT
7	+24 VDC	10	NA
8	DC GND	11	AC-
9	EG	12	AC+

TITLE:
POWER DISTRIBUTION ASSEMBLIES #2 & #3
SHEET 1 OF 3

NO SCALE

TEES 2008

A6-12



TITLE: POWER DITRIBUTION ASSEMBLIES
#2 & #3
SHEET 2 OF 3

NO SCALE

TEES 2008

A6-13

POWER DISTRIBUTION ASSEMBLY TERMINAL BLOCK ASSIGNMENT DETAIL

BLOCK	T1	T2		T3	T4	
PDA's	2A/B (3A/B-NA)	2A/B	3A/B	2 & 3A/B	2A/B	3A/B
POS						
1	EG BUS/EG	*/ER AC-	EG BUS/EQ GND	+24 VDC BUS/PS-7	NA /NA	FL1/SP 3-3
2	AC- BUS/AC-	01-5/FU1-7	AC- BUS/AC-	NA /PS-7	NA /NA	FL2/SP 3-5
3	AC- BUS/AC-	01-6/FU1-8	* /MCB (SEC)	DC GND BUS/PS-8	NA /NA	FL3/SP 3-7
4	03-5 /SCB CKT 5	01-7/FU2-7	* /MCB (SEC)	NA /PS-8	NA /NA	FL4/SP 2-3
5	* /MCB (SEC)	01-8/FU2-8	* /MU		NA /NA	FL5/SP 2-5
6	* /MCB (SEC)	* /TR NC CKT	* /TR COIL		NA /NA	FL6/SP 2-7
7	* /SSR	01-1/SCB CKT 1	NA /TRC2NO		NA /NA	FL7/SP 1-3
8	03-6 /SCB CKT 6	01-2/SCB CKT 2	NA /TRC2NC		NA /NA	FL8/SP 1-5
9	* /MCB (SEC)	01-3/SCB CKT 3	03-5 /FLD2		NA /NA	FL9/SP 1-7
10	* /ER AC+	01-4/SCB CKT 4	NA /NA		NA /NA	NA /NA

A = EXTERNAL SIDE B = INTERNAL SIDE * = WIRE PER ONE LINE DIAGRAM

NOTES (for details A6-11: to A6-13)

1. SHEET DIFINITIONS:
   - CKT = CIRCUIT
   - FLD1 = FIELD 1
   - FU1-7 = FLASHER UNIT #1, PIN 7
   - L = LAMP
   - SSR = SOLID STATE RELAY
   - MN = MAIN
   - OD = OUTSIDE DIMENSION
   - PS-7 = POWER SUPPLY PIN 7
   - SP 3-3 = SWITCH PACK 3, PIN 3
   - 01-8 = OUTPUT FILE TB 01, POSITION 8
   - EG = EQUIPMENT GROUND
   - CIRCUIT BREAKER FL1 = FIELD LOAD 1
   - ER = EQUIPMENT RECEPTACLE
   - LD CKT#1 = LOAD CIRCUIT 1
   - MCB = MAIN CIRCUIT BREAKER
   - MU-22 = MONITOR UNIT - PIN 22
   - POS = POSITION
   - SCB = SIGNAL CIRCUIT BREAKER
   - TR = TRANSFER RELAY

2. 'U' SHAPED ROD HANDLE FABRICATED OF (0.25+/-0.05)in DIAMETER, ALUMINUM STOCK, WITH (4+/-0.125)in LENGTH, & ROD CENTER TO CENTER, SHALL BE PROVIDED. THE HANDLE SHALL BE VERTICALLY CENTERED. THE DEPTH FROM THE VERTICAL CENTERLINE OF THE HANDLE ROD TO THE MODULE FRONT PANEL SHALL BE (1.25+/-0.125)in.

3. THE POWER SUPPLY MODULE DIMENSION, FROM FRONT PANEL TO CONNECTOR PLUG, SHALL BE (7.375+0.0, -0.125)in.

4. THUMB SCREW DEVICE.

5. A STANDARD 8-32 METAL STUD RETAINING SCREW SHALL PROVIDE PROPER SECRING OF THE POWER SUPPLY WHEN INSTALLED IN THE PDA USING WASHERS AND A WINGNUT. WHEN TORQUED IN THE LOCKING POSITION NO STRESS SHALL BE APPLIED ON THE MATING SOCKET/PLUG CONNECTOR SURFACE. NO MOUNTING OF CHASSIS SUPPORT SCREWS SHALL PROTRUDE BEYOND THE MATING SURFACE OF THE POWER SUPPLY CONNECTOR.

6. TOP OF THE TRANSFER RELAY SHALL BE PLUSH WITH THE FRONT OF THE PDA #1 ASSEMBLY. RELAY IN PDA #2 & 3 SHALL EXTEND NO MORE THAN 1in OUT FROM THE ASSEMBLY FRONT FACE.

7. SLACK SHALL BE PROVIDED IN THE WIRING FOR THE CIRCUIT BREAKERS AND GFI RECEPTACLE TO ALLOW FOR THE REMOVAL AND REPAIR. EXCESS BENDS & STRESS ON THE WIRING SHALL BE MINIMIZED.

8. SEE OUTPUT FILE PLAN SHEET FOR HEAVY DUTY RELAY AND SWITCH PACK WIRING ASSIGNMENTS AND CONNECTOR MOUNTING LOCATION.

9. WIRING SHALL BE ROUTED (WITH EXTRA LENGTH) TO MINIMIZE MOVEMENT WHEN FRONT PANEL DOOR IS OPENED. THE WIRING GOING TO THE FRONT PANEL SHALL BE ROUTED SUCH THAT IT DOES NOT CAUSE UNDUE TWISTING OR BENDING OF THE WIRES.

10. NO VENTILATION HOLE SHALL BE LARGE ENOUGH TO PLACE A 0.375in DIAMETER OPJECT THROUGH.

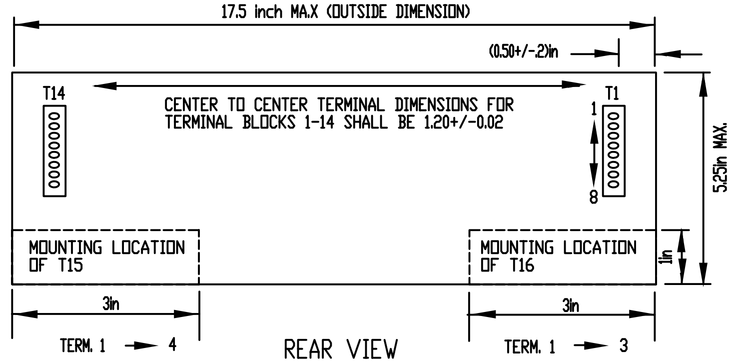
11. THE C5P SUPPORT CONNECTOR AND SUPPORT BRACKET SHALL BE INSTALLED(WIRING N/A) IN THE PDA #2. IF PDA #2 IS USED, THE INPUT PANEL C5P CONNECTOR IS NOT REQUIRED AND HARNESS #2 - C5P. THE C6P CONNECTOR AND SUPPORT BRACKET SHALL BE INSTALLED IN PDA #3.

TITLE:
POWER DISTRIBUTION ASSEMBLIES #2 & #3
SHEET 3 OF 3

NO SCALE

TEES 2008

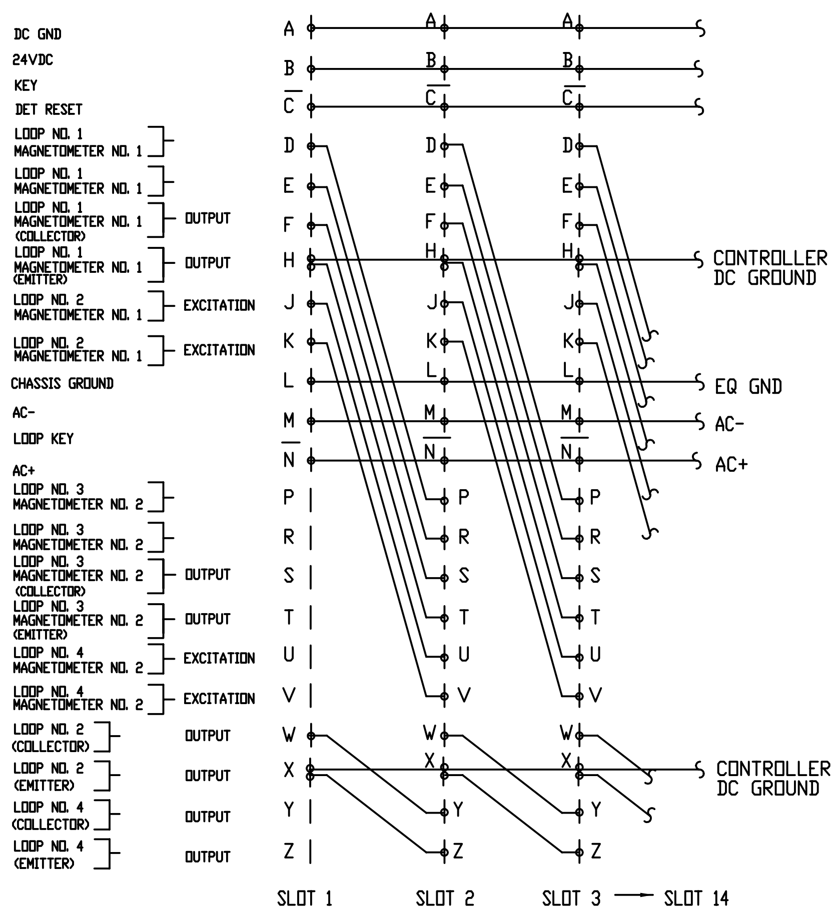
INPUT FILE DETAIL



INPUT FILE TERMINAL ASSIGNMENT DETAIL

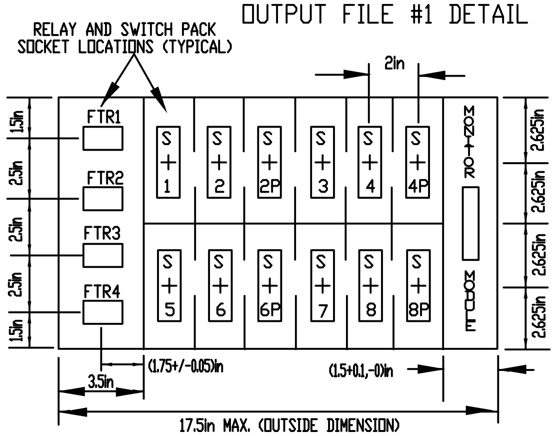
T1-14 Term	T1-14 Pin - Function	T15 Term	T15 Function	T16 Term	T16 Function
1	SP- Spare				
2	F - Channel 1 Output	1	+24 VDC	1	AC+
3	W - Channel 2 Output	2	DC Ground	2	AC-
4	D - Channel 1 Input	3	Det Reset	3	Equip. Ground
5	E - Channel 1 Input	4	C1 Harness DC Ground		
6	J - Channel 2 Input				
7	K - Channel 2 Input				
8	L - Equip. Ground				

INPUT FILE WIRING DIAGRAM

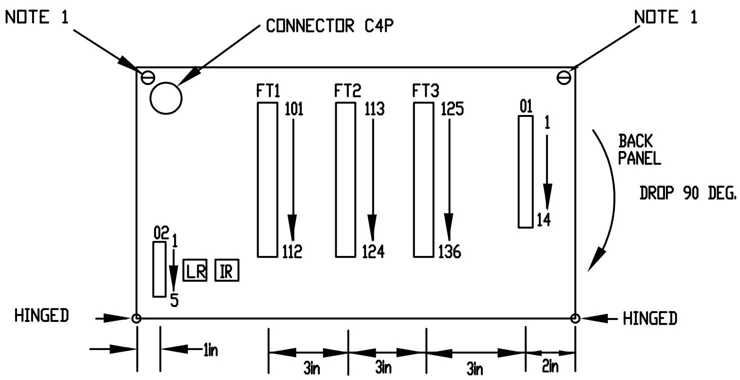


TITLE: INPUT FILES	
SHEET 1 OF 5	
NO SCALE	A6-15
TEES 2008	

OUTPUT FILE #1 DETAIL

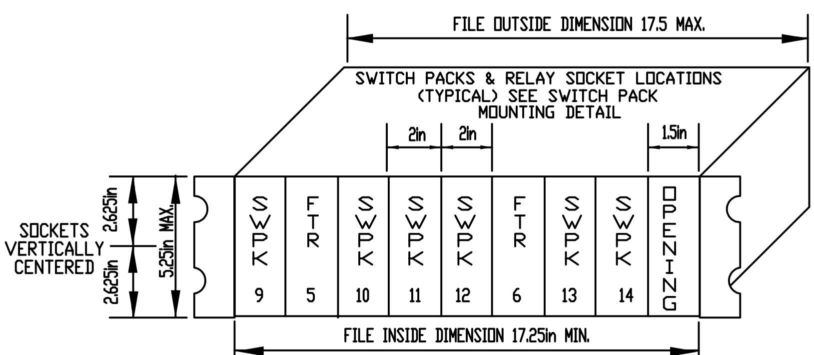


FRONT VIEW

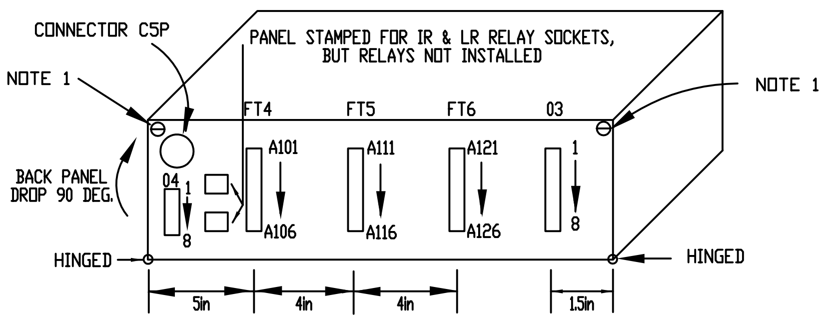


REAR VIEW
(BACK PANEL)

OUTPUT FILE #2 DETAIL



FRONT VIEW



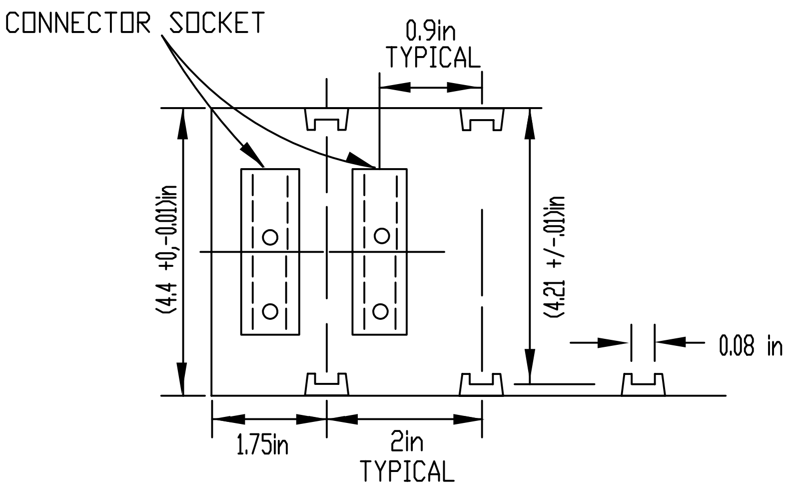
REAR VIEW
(BACK PANEL)

NOTE:

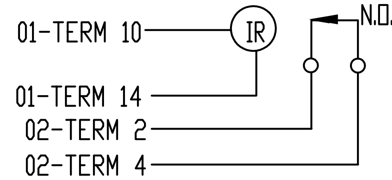
1. Thumb screw device.

TITLE: OUTPUT FILES SHEET 2 OF 5	
NO SCALE	A6-16
TEES 2008	

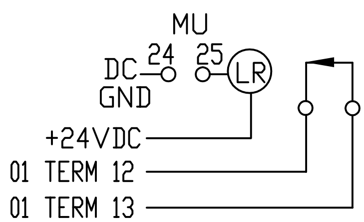
SWITCH PACK MOUNTING DETAIL



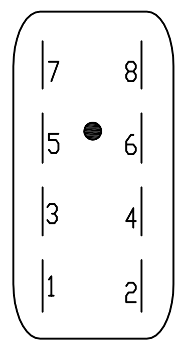
ISOLATION RELAY (IR) DETAIL



LOGIC RELAY (LR) DETAIL



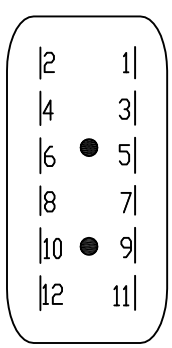
HEAVY DUTY RELAY SOCKET DETAIL



REAR VIEW

PIN	FUNCTION
1	COIL
2	COIL
3	N.C. CIRCUIT #1
4	N.C. CIRCUIT #2
5	COMMON CIRCUIT #1
6	COMMON CIRCUIT #2
7	N.O. CIRCUIT #1
8	N.O. CIRCUIT #2

SWITCH PACK SOCKET DETAIL



REAR VIEW

PIN	FUNCTION
1	AC+
2	EQUIP. GROUND
3	RED OUTPUT
4	NA
5	YELLOW OUTPUT
6	RED INPUT
7	GREEN OUTPUT
8	YELLOW INPUT
9	+24 VDC
10	GREEN INPUT
11	NA
12	NA

TITLE: INPUT & OUTPUT FILES

SHEET 3 OF 5

NO SCALE

TEES 2008

A6-17

OUTPUT FILE #1 TERMINAL ASSIGNMENT DETAIL

01

TERM	FUNCTION
1	PDA CKT1/SWPKS 1,2,2P-1
2	PDA CKT2/SWPKS 3,4,4P-1
3	PDA CKT3/SWPKS 5,6,6P-1
4	PDA CKT4/SWPKS 7,8,8P-1
5	PDA FU1 CKT1/FTR1
6	PDA FU1 CKT2/FTR2
7	PDA FU2 CKT1/FTR3
8	PDA FU2 CKT2/FTR4
9	EQUIP. GROUND
10	AC-
11	AC+ (FROM PDA)
12	SSR (TO PDA)
13	DOOR SW (FROM POL PAN)
14	FTR COILS (TO)

02

TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	1F1-14J, STOPTIME (FROM MU)
4	1F1-14D FLASH SENSE (FROM IR)
5	EXTERNAL RESET (TO MU)

FT1

TERM	FUNCTION
101	SWPK 4-RED
102	SWPK 4-YEL
103	SWPK 4-GRN
104	SWPK 4P-RED
105	SWPK 4P-YEL
106	SWPK 4P-GRN
107	SWPK 8-RED
108	SWPK 8-YEL
109	SWPK 8-GRN
110	SWPK 8P-RED
111	SWPK 8P-YEL
112	SWPK 8P-GRN

FT2

TERM	FUNCTION
113	SWPK 2P-RED
114	SWPK 2P-YEL
115	SWPK 2P-GRN
116	SWPK 3-RED
117	SWPK 3-YEL
118	SWPK 3-GRN
119	SWPK 6P-RED
120	SWPK 6P-YEL
121	SWPK 6P-GRN
122	SWPK 7-RED
123	SWPK 7-YEL
124	SWPK 7-GRN

FT3

TERM	FUNCTION
125	SWPK 1-RED
126	SWPK 1-YEL
127	SWPK 1-GRN
128	SWPK 2-RED
129	SWPK 2-YEL
130	SWPK 2-GRN
131	SWPK 5-RED
132	SWPK 5-YEL
133	SWPK 5-GRN
134	SWPK 6-RED
135	SWPK 6-YEL
136	SWPK 6-GRN

OUTPUT FILE #2 TERMINAL ASSIGNMENT DETAIL

03

TERM	FUNCTION
1	PDA FU1 CKT1/FTR5
2	PDA FU2 CKT2/FTR6
3	PDA FTR COILS (TO)
4	AC-
5	PDA CKT5/SWPKS 9,10,11-1
6	PDA CKT6/SWPKS 12,13,14-1
7	EQUIP. GROUND
8	AC+ (FROM PDA)

04

TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	STOPTIME
4	FLASH SENSE
5	EXTERNAL RESET
6	WDT INPUT
7	LR COIL (UNIT IN)
8	SSR

FT4

TERM	FUNCTION
A101	SWPK 13-RED
A102	SWPK 13-YEL
A103	SWPK 13-GRN
A104	SWPK 14-RED
A105	SWPK 14-YEL
A106	SWPK 14-GRN

FT5

TERM	FUNCTION
A111	SWPK 11-RED
A112	SWPK 11-YEL
A113	SWPK 11-GRN
A114	SWPK 12-RED
A115	SWPK 12-YEL
A116	SWPK 12-GRN

FT6

TERM	FUNCTION
A121	SWPK 9-RED
A122	SWPK 9-YEL
A123	SWPK 9-GRN
A124	SWPK 10-RED
A125	SWPK 10-YEL
A126	SWPK 10-GRN

TITLE: OUTPUT FILES #1 & #2

SHEET 4 OF 5

NO SCALE

TEES 2008

A6-18

MODEL 210 MONITOR UNIT PIN ASSIGNMENT

CONNECTOR PIN NO.	MONITOR FUNCTION	TERMINATION	CONNECTOR PIN NO.	MONITOR FUNCTION	TERMINATION
1	SWPKS 2 GRN		A	SWPKS 2 YEL	
2	SWPKS 2P GRN		B	SWPKS 6 GRN	
3	SWPKS 6 YEL		C	SWPKS 6P GRN	
4	SWPKS 4 GRN		D	SWPKS 4 YEL	
5	SWPKS 4P GRN		E	SWPKS 8 GRN	
6	SWPKS 8 YEL		F	SWPKS 8P GRN	
7	SWPKS 5 GRN		H	SWPKS 5 YEL	
8	T & B		J	SWPKS 8 GRN	
9	SWPKS 1 YEL		K	T & B	
10	SWPKS 7 GRN		L	SWPKS 7 YEL	
11	T & B		M	SWPKS 3 GRN	
12	SWPKS 3 YEL		N	T & B	
13	T & B		P	NA	
14	NA		R	T & B	
15	T & B		S	T & B	
16	T & B		T	NA	
17	NA		U	T & B	
18	T & B		V	T & B	
19	NA		W	NA	
20	EQUIP. GROUND	01-TERM 9	X	NA	
21	AC-	01-TERM 10	Y	DC GROUND	02-TERM 2
22	WATCHDOG TIMER	C4-37	Z	EXTERNAL RESET	02-TERM 5
23	+24 VDC	02-TERM 1	AA	T & B	
24	B.D. OUT CKT	LOGIC RELAY COIL	BB	STOPTIME	02-TERM 5
25	B.D. OUT CKT	DC GROUND	CC	NA	DC GROUND
26	NA		DD	NA	
27	NA		EE	OUTPUT-SW SIDE 2	01-TERM 12
28	OUTPUT-SW SIDE 1	AC+	FF	AC+	01-TERM 11

NOTES: (for details A6-14 to A6-18)

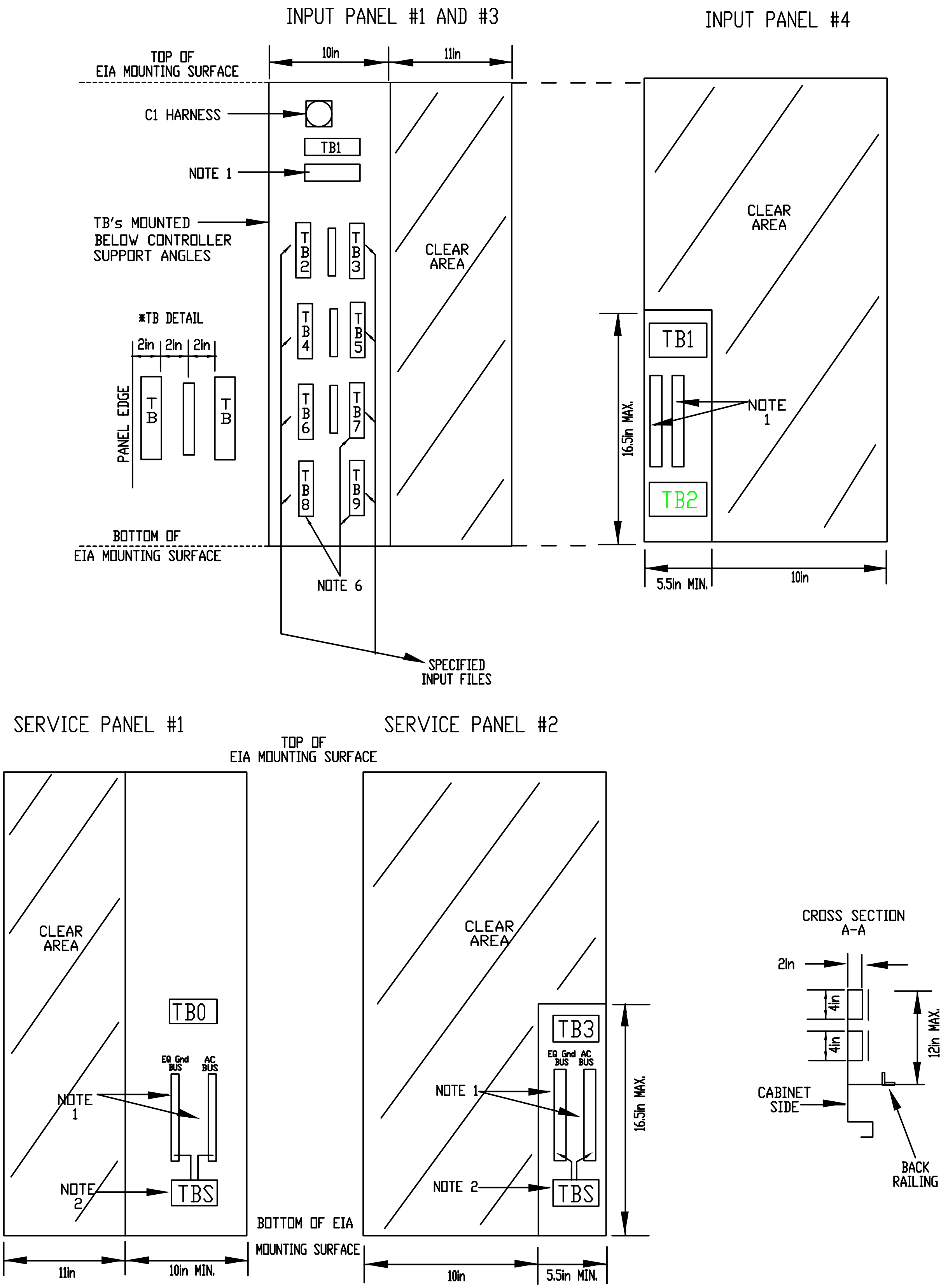
1. TOP OF RELAYS SHALL BE FLUSH WITH FACE OF FILE.
2. THE ISOLATION RELAY SHALL BE POTTER & BRUMFIELD R10-E1-X2-115 (OR EQUAL). THE LOGIC RELAY (LR) SHALL BE A POTTER AND BRUMFIELD KUP11(D11 OR 15) OR EQUAL.
3. SEE CONNECTORS C4 & C5 WIRING LISTS FOR CONNECTOR/FILE INTERFACE
4. SHEET DEFINITIONS:
   CKT = CIRCUIT
   FU = FLASHER UNIT
   FTR = FLASH TRANSFER RELAY
   IFI-14D = INPUT FILE "I", TB 14, TERMINAL D
   SSR = SOLID STATE RELAY
   MU = MONITOR UNIT
   N.C. = NORMALLY CLOSED RELAY CIRCUIT
   N.O = NORMALLY OPEN RELAY CIRCUIT
   PDA FU1 CKT1 = PDA FLAHSER UNIT 1, OUTPUT CIRCUIT 1
   POL PAN = POLICE PANEL
   SW = SWITCH
   SWPK(S) = SWITCH PACK(S)
   T&B = CONDUCTORS CONNECTED TO PIN,
   TWO FEET IN LENGTH WITH
   RING LUG ON UNCONNECTED END,
   TIED AND BUNDLED SEPARATELY
   2P-1 = PHASE 2 PED. PIN

TITLE: MODEL 210 MONITOR UNIT PIN ASSIGNMENT

NO SCALE

TEES 2008

A6-19



TITLE: SIDE PANELS SHEET 1 OF 3	
NO SCALE	A6-20
TEES 2008	

INPUT PANEL #1 TERMINAL BLOCK ASSIGNMENT DETAIL

POS	A	B
TB1 – * SEE INPUT PANEL #4 TB1 ASSIGNMENTS		

POS	A	B
TB2-1	DET 1	I-1D
2		I-1E
3	DET 2	I-1J
4		I-1K
5	DET 3	I-2D
6		I-2E
7	DET 4	I-2J
8		I-2K
9	DET 5	I-3D
10		I-3E
11	DET 6	I-3J
12		I-3K

POS	A	B
TB3-1	DET 19	J-1D
2		J-1E
3	DET 20	J-1J
4		J-1K
5	DET 21	J-2D
6		J-2E
7	DET 22	J-2J
8		J-2K
9	DET 23	J-3D
10		J-3E
11	DET 24	J-3J
12		J-3K

POS	A	B
TB4-1	DET 7	I-4D
2		I-4E
3	DET 8	I-4J
4		I-4K
5	DET 9	I-5D
6		I-5E
7	DET 10	I-5J
8		I-5K
9	DET 11	I-6D
10		I-6E
11	DET 12	I-6J
12		I-6K

POS	A	B
TB5-1	DET 25	J-4D
2		J-4E
3	DET 26	J-4J
4		J-4K
5	DET 29	J-5D
6		J-5E
7	DET 30	J-5J
8		J-5K
9	DET 31	J-6D
10		J-6E
11	DET 32	J-6J
12		J-6K

POS	A	B
TB6-1	DET 13	I-7D
2		I-7E
3	DET 14	I-7J
4		I-7K
5	DET 15	I-8D
6		I-8E
7	DET 16	I-8J
8		I-8K
9	DET 17	I-9D
10		I-9E
11	DET 18	I-9J
12		I-9K

POS	A	B
TB7-1	DET 33	J-7D
2		J-7E
3	DET 34	J-7J
4		J-7K
5	DET 35	J-8D
6		J-8E
7	DET 36	J-8J
8		J-8K
9	DET 37	J-9D
10		J-9E
11	DET 38	J-9J
12		J-9K

POS	A	B
TB8-1	MANUAL	I-11D
2	SPARE	I-11J
3	11COM	I-11K
4	PED02	I-12D
5	PED04	I-12J
6	12COM	I-12K
7	PED06	I-13D
8	PED08	I-13J
9	13COM	I-13K
10	FLH SENSE	I-14K
11	STOP	I-14J
12	14COM	I-14K

POS	A	B
TB9-1	SPARE2	I-11D
2	SPARE3	I-11J
3	11COM	I-11K
4	EVA	I-12D
5	EVC	I-12J
6	12COM	I-12K
7	EVB	I-13D
8	EVD	I-13J
9	13COM	I-13K
10	RR1	I-14K
11	RR2	I-14J
12	14COM	I-14K

INPUT PANEL #3 TERMINAL BLOCK ASSIGNMENT DETAIL

POSITION	A	B
TB1-1	+24VDC	IF,C5
2	+24VDC	PDA
3	*SEE INPUT PANEL	
4	TB1 PINS 2 TO 6	
5	ASSIGNMENTS	

POSITION	A	B
TB3-1	DET 7	I-4D
2		I-4E
3	DET 8	I-4J
4		I-4K
5	DET 9	I-5D
6		I-5E
7	DET 10	I-5J
8		I-5K
9	DET 11	I-6D
10		I-6E
11	DET 12	I-6J
12		I-6K

POSITION	A	B
TB5-1	DET 19	I-10D
2		I-10E
3	DET 20	I-10J
4		I-10K
5	DET 21	I-11D
6		I-11E
7	DET 22	I-11J
8		I-11K
9	DET 23	I-12D
10		I-12E
11	DET 24	I-12J
12		I-12K

POSITION	A	B
TB2-1	DET 1	I-1D
2		I-1E
3	DET 2	I-1J
4		I-1K
5	DET 3	I-2D
6		I-2E
7	DET 4	I-2J
8		I-2K
9	DET 5	I-3D
10		I-3E
11	DET 6	I-3J
12		I-3K

POSITION	A	B
TB4-1	DET 13	I-7D
2		I-7E
3	DET 14	I-7J
4		I-7K
5	DET 15	I-8D
6		I-8E
7	DET 16	I-8J
8		I-8K
9	DET 17	I-9D
10		I-9E
11	DET 18	I-9J
12		I-9K

POSITION	A	B
TB6-1	DET 25	I-13D
2		I-13E
3	DET 26	I-13J
4		I-13K
5	DET 27	I-14D
6		I-14E
7	DET 28	I-14J
8		I-14K
9	NA	I-NA
10	NA	I-NA
11	NA	I-NA
12	NA	I-NA

INPUT PANEL #4 TERMINAL BLOCK ASSIGNMENT DETAIL

TERM	A	B
TB1-1	+24VDC	OF IF M
-2	M RESET	NA
-3	RESERVED	RESERVED (COMM IN)
-4	RESERVED	RESERVED (COMM IN)
-5	RESERVED	RESERVED (COMM OUT)
-6	RESERVED	RESERVED (COMM OUT)
TB2-1 TO 6	NA	NA

TITLE: SIDE PANELS

SHEET 2 OF 3

NO SCALE

TEES 2008

A6-21

SERVICE PANELS 1 & 2
TERMINAL BLOCK ASSIGNMENT DETAIL

TERM	A	B
SPA-1	AC+	TO MAIN CIRCUIT BREAKER IN PDA
SPA-2	NA	EQUIPMENT GROUND (EQ. GND) BUS
SPA-3	AC-	AC- BUS
TB0-1 TO 12	NA	NA
TB3-1 TO 6	NA	NA

TB1 TERMINAL BLOCK

POS	SIDE A	SIDE B	C10 CONNECTOR PINS
1	+24 VDC (PDA3)	I/O FILES	
2	+24 VDC (POS 1)	CAB HARNESS #5	13, 14
3-7	DC GRD (PDA 3)	C1 PINS 1 & 104, I/O FILES & CAB HARNESS #5	15, 16
8-11	NA	NA	
12,13	CM1	CAB HARNESS #5	1,2
14,15	CM2	CAB HARNESS #5	3,4
16,17	CM3	CAB HARNESS #5	5,6
18,19	CM4	CAB HARNESS #5	7,8
20,21	PHOTO CELL	CAB HARNESS #5	9,10
22	C1 PIN 10	CIA CONTROL 4	11
23	C1 PIN 18	NA	
24	C1 PIN 63	NA	
25	C1 PIN 64	NA	
26	C1 PIN 65	POLICE CONTROL	
27	C1 PIN 66	POLICE LIGHTS	
28	C1 PIN 77	NA	
29	NA	NA	
30	NA	NA	

NOTES: (for details A6-19 to A6-21):

1. 10 TERMINAL (#8 WIRE) MINIMUM COPPER BUS.

2. THE TERMINAL BLOCKS SHALL HAVE TERMINAL POSITIONS NECESSARY TO MATCH POSITION ASSIGNMENTS. TERMINAL POSITION SCREWS SHALL BE 8-32 EXCEPT FOR SPA, TB0 & TB3, WHICH SHALL BE 10-32.

3. SHEETS DEFINITIONS:
   11 COM = DC COMMON
   COMM = COMMUNICATION
   DET1 = DETECTOR #1
   EVA = EMERGENCY VEHICLE PREEMPTION A
   IFI-1D = INPUT FILE I, SLOT 1, CONNECTOR PIN D
   OF = OUTPUT FILE
   M = MONITOR MODULE
   NA = NOT ASSIGNED
   RR1 = RAILROAD PREEMPTION 1

4. INPUT PANEL #3 SHALL BE PUNCHED & TAPPED FOR TB 7, 8 & 9 BUT NOT SUPPLIED.

5. A 4-ft LENGTH "CMS" HARNESS OF 14 #20 (OR LARGER) CONDUCTORS SHALL BE FURNISHED AND INSTALLED IN THE CABINET. ONE END OF THE HARNESS SHALL BE THE C10S CONNECTOR RESTING IN C10P (MOUNTED ON THE INPUT PANEL #3) WHEN NOT IN USE. THE OTHER END SHALL BE STRIPPED (ACCORDING TO MANUFACTURERS REQUIREMENTS) & CONNECTED TO THE "B SIDE" OF TB1. THE CONDUCTOR BUNDLE SHALL HAVE EXTERNAL PROTECTION. PIN AND POSITION ASSIGNMENTS ARE AS FOLLOWS OF THE TB1 & C10 CONNECTORS".

TITLE: SIDE PANELS SHEET 3 OF 3	
NO SCALE	A6-22
TEES 2008	

G1 HARNESS #1 WIRING LIST

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC-GND	DC-GND BUS	-	27	04-1	C4-25	SWPK 6P-RED
2	01-1	C4-1	SWPK 4P-RED	28	04-2	C4-26	SWPK 6P-GRN
3	01-2	C4-2	SWPK 4P-GRN	29	04-3	C4-27	SWPK 6-RED
4	01-3	C4-3	SWPK 4-RED	30	04-4	C4-28	SWPK 6-YEL
5	01-4	C4-4	SWPK 4-YEL	31	04-5	C4-29	SWPK 6-GRN
6	01-5	C4-5	SWPK 4-GRN	32	04-6	C4-30	SWPK 5-RED
7	01-6	C4-6	SWPK 3-RED	33	04-7	C4-31	SWPK 5-YEL
8	01-7	C4-7	SWPK 3-YEL	34	04-8	C4-32	SWPK 5-GRN
9	01-8	C4-8	SWPK 3-GRN	35	05-1	C4-33	SWPK 2P-YEL
10	02-1	C4-9	SWPK 2P-RED	36	05-2	C4-34	SWPK 6P-YEL
11	02-2	C4-10	SWPK 2P-GRN	37	05-3	C4-35	SWPK 4P-YEL
12	02-3	C4-11	SWPK 2-RED	38	05-4	C4-36	SWPK 8P-YEL
13	02-4	C4-1	SWPK 2-YEL	39	I1-1	IFI-2F	2 CE
14	DC GND	IFI-15-4	INPUT DC GND	40	I1-2	IFJ-2F	6 CE
15	02-5	C4-13	SWPK 2-GRN	41	I1-3	IFI-6F	4 CE
16	02-6	C4-14	SWPK 1-RED	42	I1-4	IFJ-6F	8 CE
17	02-7	C4-15	SWPK 1-YEL	43	I1-5	IFI-2W	2 CE
18	02-8	C4-16	SWPK 1-GRN	44	I1-6	IFJ-2W	6 CE
19	03-1	C4-17	SWPK 8P-RED	45	I1-7	IFI-6W	4 CE
20	03-2	C4-18	SWPK 8P-GRN	46	I1-8	IFJ-6W	8 CE
21	03-3	C4-19	SWPK 8-RED	47	I2-1	IFI-4F&W	2 CALL
22	03-4	C4-20	SWPK 8-YEL	48	I2-2	IFJ-4F&W	6 CALL
23	03-5	C4-21	SWPK 8-GRN	49	I2-3	IFI-8F&W	4 CALL
24	03-6	C4-22	SWPK 7-RED	50	I2-4	IFJ-8F&W	8 CALL
25	03-7	C4-23	SWPK 7-YEL	51	I2-5	IFJ-14F	RR1 PREEMPT
26	03-8	C4-24	SWPK 7-GRN	52	I2-6	IFJ-14	RR2 PREEMPT

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
53	12-7	IFI-11W	SPARE #1	79	16-5	IFJ-7W	8 CE
54	12-8	IFJ-11F	SPARE #2	80	16-6	IFI-11F	ADVANCE
55	13-1	IFJ-1F&W	5 CE	81	16-7	IFI-14F	FLASH SENSE
56	13-2	IFI-1F&W	1 CE	82	16-8	IFI-14W	STOP TIME
57	13-3	IFJ-5F&W	7 CE	83	06-1	C5-1	SWPK 14-RED
58	13-4	IFI-5F&W	3 CE	84	06-2	C5-2	SWPK 14-GRN
59	13-5	IFJ-9F	5 CE	85	06-3	C5-3	SWPK 13-RED
60	13-6	IFI-9F	1 CE	86	06-4	C5-4	SWPK 13-YEL
61	13-7	IFJ-9W	7 CE	87	06-5	C5-5	SWPK 13-GRN
62	13-8	IFI-9W	3 CE	88	06-6	C5-6	SWPK 12-RED
63	14-5	IFI-3F	2 CE	89	06-7	C5-7	SWPK 12-YEL
64	14-6	IFJ-3F	6 CE	90	06-8	C5-8	SWPK 12-GRN
65	14-7	IFI-7F	4 CE	91	07-1	C5-9	SWPK 11-RED
66	14-8	IFJ-7F	8 CE	92	DC-GND	DC GND BUS	-
67	15-1	IFI-12F	2 PED	93	07-2	C5-10	SWPK 11-GRN
68	15-2	IFI-13F	6 PED	94	07-3	C5-11	SWPK 10-RED
69	15-3	IFI-12W	4 PED	95	07-5	C5-12	SWPK 10-YEL
70	15-4	IFI-13W	8 PED	96	07-5	C5-13	SWPK 10-GRN
71	15-5	IFJ-12F	EVA PREEMPT	97	07-6	C5-14	SWPK 9-RED
72	15-6	IFJ-13F	EVB PREEMPT	98	07-7	C5-15	SWPK 9-YEL
73	15-7	IFJ-12W	EVC PREEMPT	99	07-8	C5-16	SWPK 9-GRN
74	15-8	IFJ-13W	EVD PREEMPT	100	05-5	C5-17	SWPK 14-YEL
75	16-1	IFJ-11W	SPARE #3	101	05-6	C5-18	SWPK 11-YEL
76	16-2	IFI-3W	2 CE	102	05-7	IFI&J-15-3	DETECTOR RESET
77	16-3	IFJ-3W	6 CE	103	05-8	C4-37	WDT-MU
78	16-4	IFI-7W	4 CE	104	DC GND	IFJ-15-4	INPUT DC GND

TITLE: HARNESS WIRING LISTS

SHEET 1 OF 6

NO SCALE

TEES 2008

A6-23

C1 HARNESS #2 WIRING LIST
(Interconnection between CABINET & CONTROLLER)

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC-GND	TB1/3-7	DC-GND BUS	27	04-1	NA	-
2	01-1	C6-1	SWPK 1-RED	28	04-2	NA	-
3	01-2	C6-2	SWPK 1-GRN	29	04-3	NA	-
4	01-3	C6-3	SWPK 2-RED	30	04-4	NA	-
5	01-4	C6-4	SWPK 2-YEL	31	04-5	NA	-
6	01-5	C6-5	SWPK 2-GRN	32	04-6	NA	-
7	01-6	C6-6	SWPK 3-RED	33	04-7	NA	-
8	01-7	C6-7	SWPK 3-YEL	34	04-8	NA	-
9	01-8	C6-8	SWPK 3-GRN	35	05-1	NA	-
10	02-1	TB1/22	CIA CONTROL 4	36	05-2	NA	-
11	02-2	C7-25	CMS CLOCK	37	05-3	C6-9	SWPK 1-YEL
12	02-3	C7-26	CMS ENABLE	38	05-4	NA	-
13	02-4	C7-27	CMS CLEAR	39	I1-1	IFI-1W	PASSAGE 1
14	DC GND	IFI-15-4	INPUT DC GND	40	I1-2	IFI-12W	PASSAGE 2
15	02-5	C7-28	CMS DIM LEVEL 1	41	I1-3	IFI-12F	DEMAND 2
16	02-6	C7-29	CMS DIM LEVEL 2	42	I1-4	IFI-13W	OFF RAMP 2
17	02-7	C7-30	CMS DIM LEVEL 3	43	I1-5	IFI-13F	QUE 2
18	02-8	TB1/23	-	44	I1-6	IFI-14W	PASSAGE 3
19	03-1	C7-9	CMS ADDRESS 1	45	I1-7	IFI-14F	DEMAND 3
20	03-2	C7-10	CMS ADDRESS 2	46	I1-8	IFI-1F	DEMAND 1
21	03-3	C7-11	CMS ADDRESS 3	47	I2-1	IFI-2W	OFF RAMP 1
22	03-4	C7-12	CMS ADDRESS 4	48	I2-2	IFI-3W	-
23	03-5	C7-13	CMS ADDRESS 5	49	I2-3	IFI-3F	-
24	03-6	C7-14	CMS ADDRESS 6	50	I2-4	IFI-2F	QUE 1
25	03-7	C7-15	CMS ADDRESS 7	51	I2-5	IFI-5F	MAIN 1
26	03-8	C7-4	CIA CONTROL 4	52	I2-6	IFI-5W	MAIN 2

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
53	12-7	IFI-11F	RATE CODE 2	79	16-5	IFI-10F	-
54	12-8	IFI-11W	RATE CODE 1	80	16-6	IFI-9W	-
55	13-1	IFI-4F	-	81	16-7	IFI-9F	-
56	13-2	IFI-4W	-	82	16-8	IFI-10W	-
57	13-3	IFI-6F	MAIN 3	83	06-1	C5-1	SWPK 14-RED
58	13-4	IFI-6W	MAIN 4	84	06-2	C5-2	SWPK 14-GRN
59	13-5	IFI-7F	MAIN 5	85	06-3	C5-3	SWPK 13-RED
60	13-6	IFI-7W	MAIN 6	86	06-4	C5-4	SWPK 13-YEL
61	13-7	IFI-8F	-	87	06-5	C5-5	SWPK 13-GRN
62	13-8	IFI-8W	-	88	06-6	C5-6	SWPK 12-RED
63	14-5	IFI-1SP	-	89	06-7	C5-7	SWPK 12-YEL
64	14-6	IFI-2SP	-	90	06-8	C5-8	SWPK 12-GRN
65	14-7	POL CONT'L SW	-	91	07-1	C5-9	SWPK 11-RED
66	14-8	POL LIGHTS SW	-	92	DC-GND	DC GND BUS	-
67	15-1	IFI-3SP	-	93	07-2	C5-10	SWPK 11-GRN
68	15-2	IFI-4SP	-	94	07-3	C5-11	SWPK 10-RED
69	15-3	IFI-5SP	-	95	07-5	C5-12	SWPK 10-YEL
70	15-4	IFI-6SP	-	96	07-5	C5-13	SWPK 10-GRN
71	15-5	IFJ-7SP	-	97	07-6	C5-14	SWPK 9-RED
72	15-6	IFJ-8SP	-	98	07-7	C5-15	SWPK 9-YEL
73	15-7	IFJ-9SP	-	99	07-8	C5-16	SWPK 9-GRN
74	15-8	IFJ-10SP	-	100	05-5	C5-17	SWPK 14-YEL
75	16-1	IFJ-11SP	-	101	05-6	C5-18	SWPK 11-YEL
76	16-2	IFI-12SP	-	102	05-7	IFI-15-3	DETECTOR RESET
77	16-3	IFJ-13SP	-	103	05-8	C6-10	WDT
78	16-4	IFI-14SP	-	104	DC GND	DC GND BUS	-

TITLE: HARNESS WIRING LISTS SHEET 2 OF 6	
NO SCALE	A6-24
TEES 2008	

C1 HARNESS #2 WIRING LIST

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC-GND	TB1/3-7	DC-GND BUS	27	04-1	C7-17	CMS DATA 1
2	01-1	C6-1	SWPK 1-RED	28	04-2	C7-18	CMS DATA 2
3	01-2	C6-2	SWPK 1-GRN	29	04-3	C7-19	CMS DATA 3
4	01-3	C6-3	SWPK 2-RED	30	04-4	C7-20	CMS DATA 4
5	01-4	C6-4	SWPK 2-YEL	31	04-5	C7-21	CMS DATA 5
6	01-5	C6-5	SWPK 2-GRN	32	04-6	C7-22	CMS DATA 6
7	01-6	C6-6	SWPK 3-RED	33	04-7	C7-23	CMS DATA 7
8	01-7	C6-7	SWPK 3-YEL	34	04-8	C7-24	CMS DATA 8
9	01-8	C6-8	SWPK 3-GRN	35	05-1	C7-1	CIA CONTROL 1
10	02-1	TB1/22	CIA CONTROL 4	36	05-2	C7-2	CIA CONTROL 2
11	02-2	C7-25	CMS CLOCK	37	05-3	C6-9	SWPK 1-YEL
12	02-3	C7-26	CMS ENABLE	38	05-4	C7-3	CIA CONTROL 3
13	02-4	C7-27	CMS CLEAR	39	I1-1	IFI-1W	PASSAGE 1
14	DC GND	IFI-15-4	INPUT DC GND	40	I1-2	IFI-12W	PASSAGE 2
15	02-5	C7-28	CMS DIM LEVEL 1	41	I1-3	IFI-12F	DEMAND 2
16	02-6	C7-29	CMS DIM LEVEL 2	42	I1-4	IFI-13W	OFF RAMP 2
17	02-7	C7-30	CMS DIM LEVEL 3	43	I1-5	IFI-13F	QUE 2
18	02-8	TB1/23	-	44	I1-6	IFI-14W	PASSAGE 3
19	03-1	C7-9	CMS ADDRESS 1	45	I1-7	IFI-14F	DEMAND 3
20	03-2	C7-10	CMS ADDRESS 2	46	I1-8	IFI-1F	DEMAND 1
21	03-3	C7-11	CMS ADDRESS 3	47	I2-1	IFI-2W	OFF RAMP 1
22	03-4	C7-12	CMS ADDRESS 4	48	I2-2	IFI-3W	MAIN 7
23	03-5	C7-13	CMS ADDRESS 5	49	I2-3	IFI-3F	MAIN 7
24	03-6	C7-14	CMS ADDRESS 6	50	I2-4	IFI-2F	QUE 1
25	03-7	C7-15	CMS ADDRESS 7	51	I2-5	IFI-5F	MAIN 1
26	03-8	C7-4	CIA CONTROL 5	52	I2-6	IFI-5W	MAIN 2

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
53	12-7	IFI-11F	RATE CODE 2	79	16-5	IFI-10F	MAIN 15
54	12-8	IFI-11W	RATE CODE 1	80	16-6	IFI-9W	MAIN 14
55	13-1	IFI-4F	MAIN 9	81	16-7	IFI-9F	MAIN 13
56	13-2	IFI-4W	MAIN 10	82	16-8	IFI-10W	MAIN 16
57	13-3	IFI-6F	MAIN 3	83	06-1	C5-1	SWPK 14-RED
58	13-4	IFI-6W	MAIN 4	84	06-2	C5-2	SWPK 14-GRN
59	13-5	IFI-7F	MAIN 5	85	06-3	C5-3	SWPK 13-RED
60	13-6	IFI-7W	MAIN 6	86	06-4	C5-4	SWPK 13-YEL
61	13-7	IFI-8F	MAIN 11	87	06-5	C5-5	SWPK 13-GRN
62	13-8	IFI-8W	MAIN 12	88	06-6	C5-6	SWPK 12-RED
63	14-5	TB1/24	MAIN 17	89	06-7	C5-7	SWPK 12-YEL
64	14-6	TB1/25	MAIN 18	90	06-8	C5-8	SWPK 12-GRN
65	14-7	TB1/26	POL CONT'L SW	91	07-1	C5-9	SWPK 11-RED
66	14-8	TB1/27	POL LIGHTS SW	92	DC-GND	TB1/3-7	-
67	15-1	C7-16	CIA SENSE 1	93	07-2	C5-10	SWPK 11-GRN
68	15-2	C7-31	CIA SENSE 2	94	07-3	C5-11	SWPK 10-RED
69	15-3	C7-32	CIA SENSE 3	95	07-5	C5-12	SWPK 10-YEL
70	15-4	C7-33	CIA SENSE 4	96	07-5	C5-13	SWPK 10-GRN
71	15-5	C7-34	CIA SENSE 5	97	07-6	C5-14	SWPK 9-RED
72	15-6	C7-35	CIA SENSE 6	98	07-7	C5-15	SWPK 9-YEL
73	15-7	C7-36	CIA SENSE 7	99	07-8	C5-16	SWPK 9-GRN
74	15-8	C7-37	CIA SENSE 8	100	05-5	C5-17	SWPK 14-YEL
75	16-1	C7-5	CMS LATCH	101	05-6	C5-18	SWPK 11-YEL
76	16-2	C7-6	PHASE FIRE	102	05-7	IFI-15-3	DETECTOR RESET
77	16-3	TB1/29	MAIN 19	103	05-8	C6-10	WDT
78	16-4	C7-8	CMS TEST REQ.	104	DC GND	TB1/3-7	DC GND BUS

NOTES: C7S CONNECTOR PIN 7 is not assigned.
TB1/26 - TERMINAL BLOCK 1 POSITION 26.

TITLE:
HARNESS WIRING LISTS
SHEET 3 OF 6

NO SCALE

TEES 2008

A6-25

C1 HARNESS #3 WIRING LIST

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC-GND	DC-GND BUS	-	27	04-1	C4-25	SWPK 6P-RED
2	01-1	C4-1	SWPK 4P-RED	28	04-2	C4-26	SWPK 6P-GRN
3	01-2	C4-2	SWPK 4P-GRN	29	04-3	C4-27	SWPK 6-RED
4	01-3	C4-3	SWPK 4-RED	30	04-4	C4-28	SWPK 6-YEL
5	01-4	C4-4	SWPK 4-YEL	31	04-5	C4-29	SWPK 6-GRN
6	01-5	C4-5	SWPK 4-GRN	32	04-6	C4-30	SWPK 5-RED
7	01-6	C4-6	SWPK 3-RED	33	04-7	C4-31	SWPK 5-YEL
8	01-7	C4-7	SWPK 3-YEL	34	04-8	C4-32	SWPK 5-GRN
9	01-8	C4-8	SWPK 3-GRN	35	05-1	C4-33	SWPK 2P-YEL
10	02-1	C4-9	SWPK 2P-RED	36	05-2	C4-34	SWPK 6P-YEL
11	02-2	C4-10	SWPK 2P-GRN	37	05-3	C4-35	SWPK 4P-YEL
12	02-3	C4-11	SWPK 2-RED	38	05-4	C4-36	SWPK 8P-YEL
13	02-4	C4-12	SWPK 2-YEL	39	I1-1	IFI-2F	2 CE
14	DC GND	IFI-15-4	INPUT DC GND	40	I1-2	IFI-6F	6 CE
15	02-5	C4-13	SWPK 2-GRN	41	I1-3	IFI-4F	4 CE
16	02-6	C4-14	SWPK 1-RED	42	I1-4	IFI-8F	8 CE
17	02-7	C4-15	SWPK 1-YEL	43	I1-5	IFI-2W	2 CE
18	02-8	C4-16	SWPK 1-GRN	44	I1-6	IFI-6W	6 CE
19	03-1	C4-17	SWPK 8P-RED	45	I1-7	IFI-4W	4 CE
20	03-2	C4-18	SWPK 8P-GRN	46	I1-8	IFI-8W	8 CE
21	03-3	C4-19	SWPK 8-RED	47	I2-1	IFI-1W	2 CALL
22	03-4	C4-20	SWPK 8-YEL	48	I2-2	IFI-5W	6 CALL
23	03-5	C4-21	SWPK 8-GRN	49	I2-3	IFI-3W	4 CALL
24	03-6	C4-22	SWPK 7-RED	50	I2-4	IFI-7W	8 CALL
25	03-7	C4-23	SWPK 7-YEL	51	I2-5	IFI-9F	RR1 PREEMPT
26	03-8	C4-24	SWPK 7-GRN	52	I2-6	IFI-9W	RR2 PREEMPT

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
53	12-7	TB2-5	SPARE #1	79	16-5	IFI-13SP	8 CE
54	12-8	TB2-6	SPARE #2	80	16-6	IFI-14SP	ADVANCE
55	13-1	IFI-5F	5 CE	81	16-7	IFI-14F	FLASH SENSE
56	13-2	IFI-1F	1 CE	82	16-8	IFI-14W	STOP TIME
57	13-3	IFI-7F	7 CE	83	06-1	NA	-
58	13-4	IFI-3F	3 CE	84	06-2	NA	-
59	13-5	IFI-1SP	-	85	06-3	NA	-
60	13-6	IFI-2SP	-	86	06-4	NA	-
61	13-7	IFI-3SP	-	87	06-5	NA	-
62	13-8	IFI-4SP	-	88	06-6	NA	-
63	14-5	IFI-5SP	-	89	06-7	NA	-
64	14-6	IFI-6SP	-	90	06-8	NA	-
65	14-7	IFI-7SP	-	91	07-1	NA	-
66	14-8	IFI-8SP	-	92	DC-GND	DC GND BUS	-
67	15-1	IFI-12F	2 PED	93	07-2	NA	-
68	15-2	IFI-13F	6 PED	94	07-3	NA	-
69	15-3	IFI-12W	4 PED	95	07-5	NA	-
70	15-4	IFI-13W	8 PED	96	07-5	NA	-
71	15-5	IFI-10F	EVA PREEMPT	97	07-6	NA	-
72	15-6	IFI-11F	EVB PREEMPT	98	07-7	NA	-
73	15-7	IFI-10W	EVC PREEMPT	99	07-8	NA	-
74	15-8	IFI-11W	EVD PREEMPT	100	05-5	NA	-
75	16-1	IFI-9SP	SPARE #3	101	05-6	NA	-
76	16-2	IFI-10SP	2 CE	102	05-7	IFI-15-3	DETECTOR RESET
77	16-3	IFI-11SP	6 CE	103	05-8	C4-37	WDT-MU
78	16-4	IFI-12SP	4 CE	104	DC GND	DC GND BUS	-

TITLE:
HARNESS WIRING LISTS
SHEET 4 OF 6

NO SCALE

TEES 2008

A6-26

C4 HARNESS #1 & #3 WIRING LIST

PIN	SOURCE	DESTINATION
1	C1-2	SWPK 4P-RED
2	C1-3	SWPK 4P-GRN
3	C1-4	SWPK 4-RED
4	C1-5	SWPK 4-YEL
5	C1-6	SWPK 4-GRN
6	C1-7	SWPK 3-RED
7	C1-8	SWPK 3-YEL
8	C1-9	SWPK 3-GRN
9	C1-10	SWPK 2P-RED
10	C1-11	SWPK 2P-GRN
11	C1-12	SWPK 2-RED
12	C1-13	SWPK 2-YEL
13	C1-15	SWPK 2-GRN
14	C1-16	SWPK 1-RED
15	C1-17	SWPK 1-YEL
16	C1-18	SWPK 1-GRN
17	C1-19	SWPK 8P-RED
18	C1-20	SWPK 8P-GRN

PIN	SOURCE	DESTINATION
19	C1-21	SWPK 8-RED
20	C1-22	SWPK 8-YEL
21	C1-23	SWPK 8-GRN
22	C1-24	SWPK 7-RED
23	C1-25	SWPK 7-YEL
24	C1-26	SWPK 7-GRN
25	C1-27	SWPK 6P-RED
26	C1-28	SWPK 6P-GRN
27	C1-29	SWPK 6-RED
28	C1-30	SWPK 6-YEL
29	C1-31	SWPK 6-GRN
30	C1-32	SWPK 5-RED
31	C1-33	SWPK 5-YEL
32	C1-34	SWPK 5-GRN
33	C1-35	SWPK 2P-YEL
34	C1-36	SWPK 6P-YEL
35	C1-37	SWPK 4P-YEL
36	C1-38	SWPK 8P-YEL
37	C1-103	SWPK WDT-MU

C5 HARNESS #1 & #2 WIRING LIST

PIN	SOURCE	DESTINATION
1	C1-83	SWPK 14-RED
2	C1-84	SWPK 14-GRN
3	C1-85	SWPK 13-RED
4	C1-86	SWPK 13-YEL
5	C1-87	SWPK 13-GRN
6	C1-77	SWPK 12-RED
7	C1-89	SWPK 12-YEL
8	C1-90	SWPK 12-GRN
9	C1-91	SWPK 11-RED
10	C1-93	SWPK 11-GRN
11	C1-94	SWPK 10-RED
12	C1-95	SWPK 10-YEL

PIN	SOURCE	DESTINATION
13	C1-96	SWPK 10-GRN
14	C1-97	SWPK 9-RED
15	C1-98	SWPK 9-YEL
16	C1-99	SWPK 9-GRN
17	C1-100	SWPK 14-YEL
18	C1-101	SWPK 11-YEL
19	NA	NA
20	NA	NA
21	NA	NA
22	NA	NA
23	NA	NA
24	+24 VDC	PIN9, ALL SOCKETS

C6 HARNESS #2 WIRING LIST

PIN	SOURCE	DESTINATION
1	C1-2	SWPK 1-RED
2	C1-3	SWPK 1-GRN
3	C1-4	SWPK 2-RED
4	C1-5	SWPK 2-YEL
5	C1-6	SWPK 2-GRN
6	C1-7	SWPK 3-RED
7	C1-8	SWPK 3-YEL
8	C1-9	SWPK 3-GRN
9	C1-37	SWPK 1-YEL
10	C1-103	WDT
11	NA	NA
12	NA	NA

PIN	SOURCE	DESTINATION
13	NA	NA
14	NA	NA
15	NA	NA
16	NA	NA
17	NA	NA
18	NA	NA
19	NA	NA
20	NA	NA
21	NA	NA
22	NA	NA
23	NA	NA
24	NA	NA

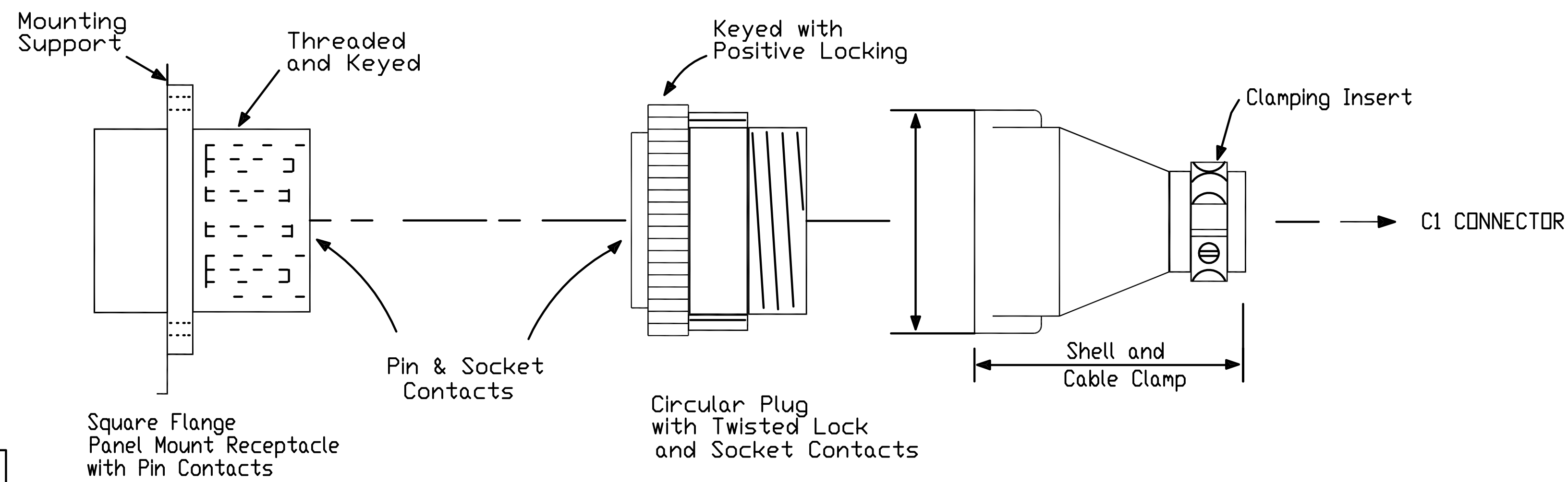
TITLE:
HARNESS WIRING LISTS
SHEET 5 OF 6

NO SCALE

TEES 2008

A6-27

CONNECTORS C4, C5 AND C6



NOTE: (for details A6-22 to A6-27)

C1-2 = CONNECTOR C1, PIN 2
EVA = EMERGENCY VEHICLE A
I1-1 = INPUT PORT 5001, BIT 1
IFI-2F, SP = INPUT FILE I, TERMINAL BLOCK 2, TERMINAL DESIGNATION F (CHANEEL 1 OUTPUT), SPARE
IFJ-6W = INPUT FILE J, TERMINAL BLOCK 6, TERMINAL DESIGNATION W (CHANNEL 2 OUTPUT)
O1-1 = OUTPUT PORT 5001, BIT 1
RR1 = RAILROAD 1
SWPK 2P-GRN = SWITCHPACK 2 PEDESTRIAN, GREEN
WDT-MU = WATCHDOG TIMER, MONITOR UNIT

2 CE = PHASE 2 COUNT & EXTENSION

TITLE: HARNESS WIRING LISTS

SHEET 6 OF 6

NO SCALE

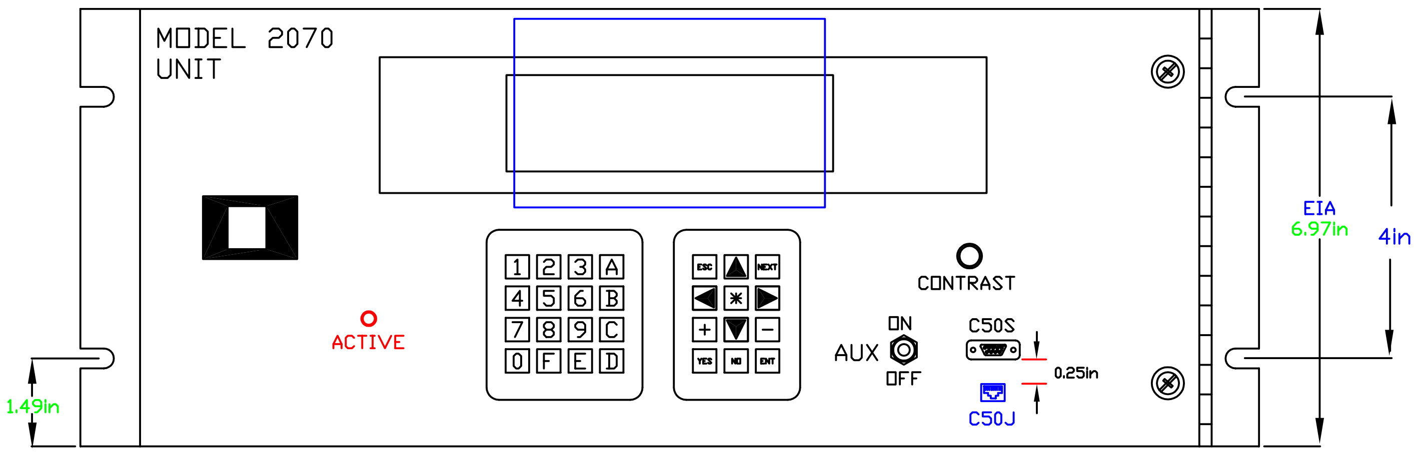
TEES 2008

A6-28

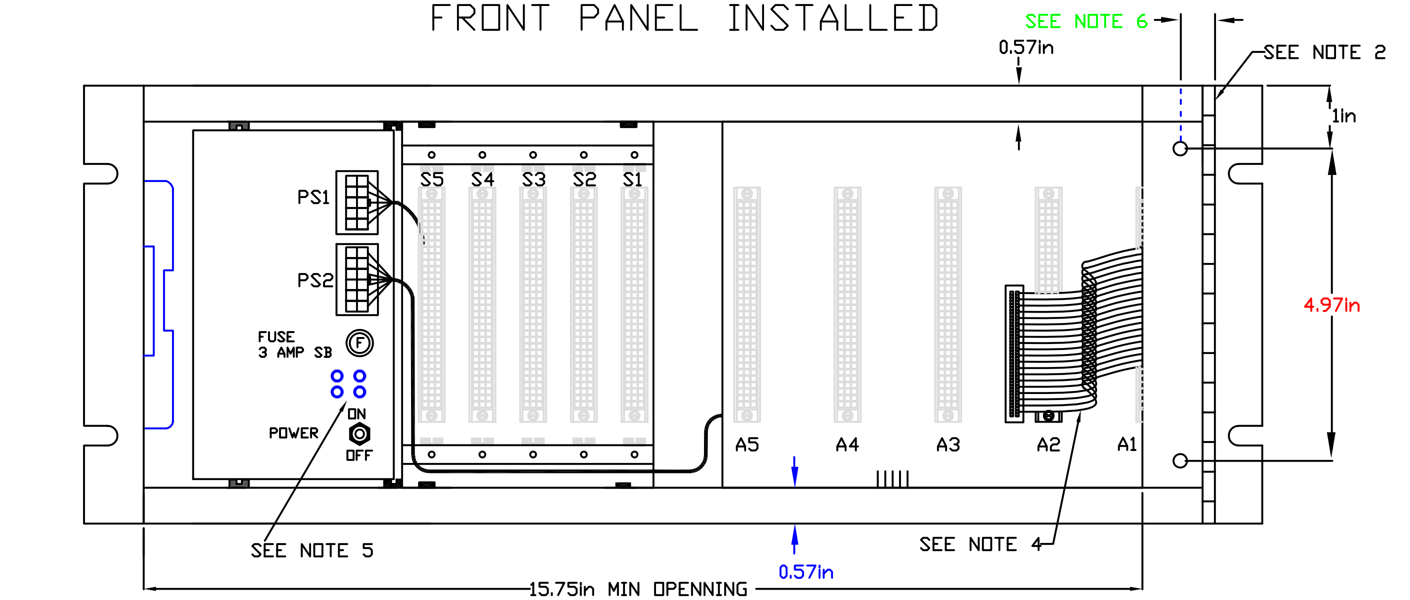
APPENDIX A7
CHAPTER 7 DETAILS

APPENDIX A8
CHAPTER 8 DETAILS

APPENDIX A9
CHAPTER 9 DETAILS



FRONT PANEL INSTALLED



FRONT PANEL REMOVED

NOTES (THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.

2. Continuous stainless steel hinge (0.157 in maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.

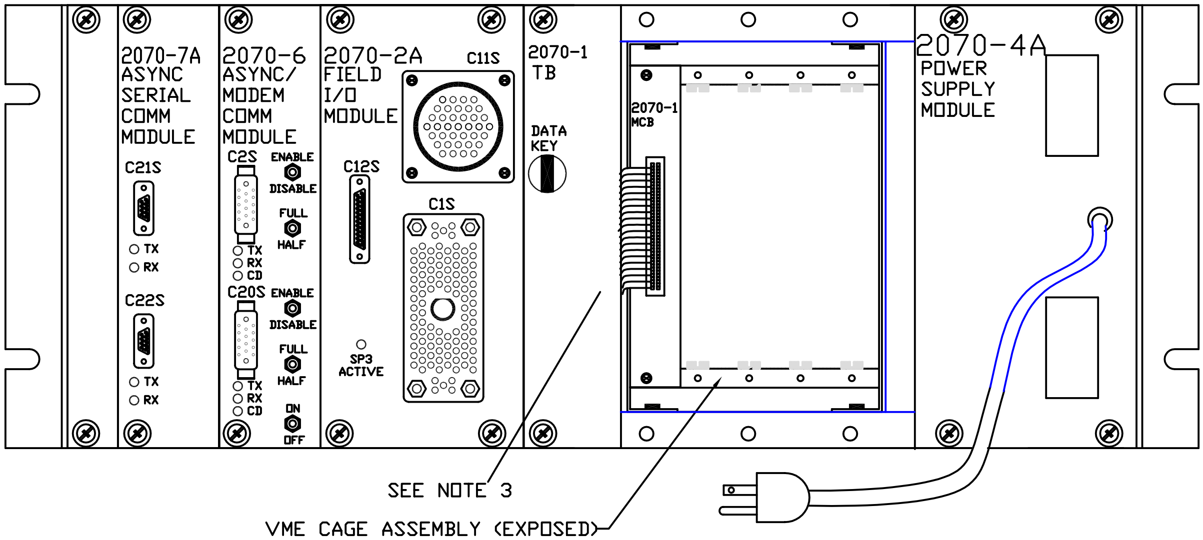
3. Actual location of ACTIVE light, AUX switch, C50S, C50J and contrast control shall be limited to ACTIVE light on the left side of the panel; AUX switch, C50S, C50J and the contrast control on the right side. They shall be located greater than 1 in from the edge of each other, other devices, connector or latch. C50J only needs to be 0.25in minimum from C50S.

4. The length of the Front Panel Harness shall be 5 in ± 2% and it shall be removeable.

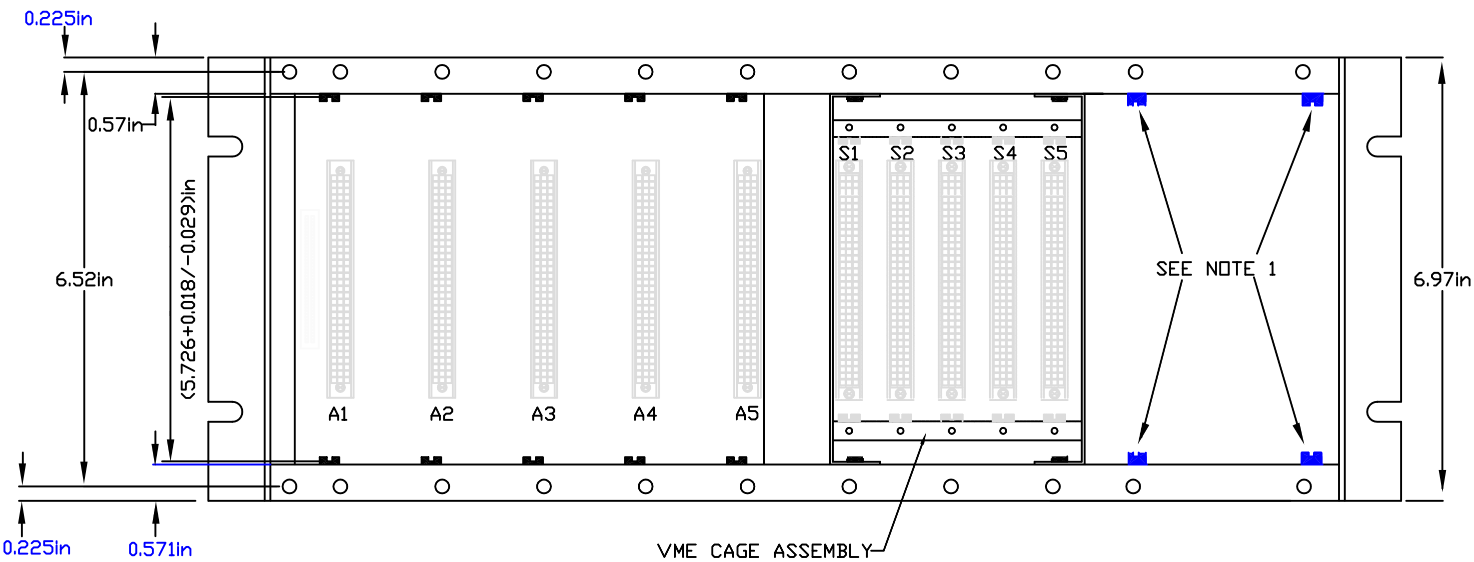
5. LED indicators for each DC voltage shall be provided.

6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside plane) shall be 0.55 in.

TITLE: MODEL 2070-CHASSIS FRONT VIEW	
NO SCALE	A9-1
TEES 2008	



REAR VIEW, LOADED



REAR VIEW, UNLOADED

NOTES (THIS DETAIL)

1. Four permanently attached 8in long Card Guides SAE 1800F (OR EQUAL) beginning 0.51in from the backplane mounting surface.

2. TB - TRANSITION BOARD
   MCB - MAIN CONTROLLER BOARD

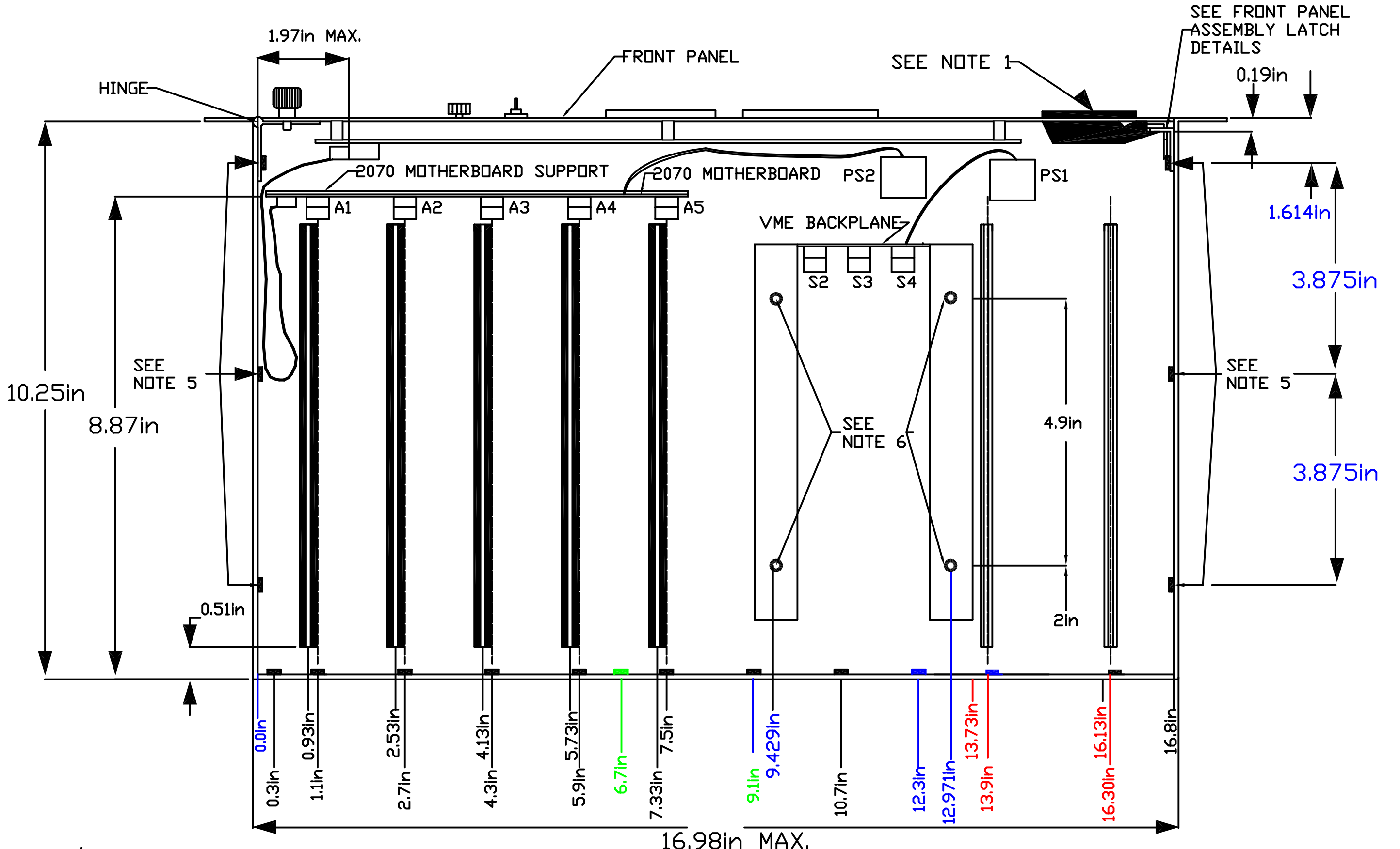
3. Maximum length of harness shall be 4in, and shall not protrude beyond the back of the 2070 unit.

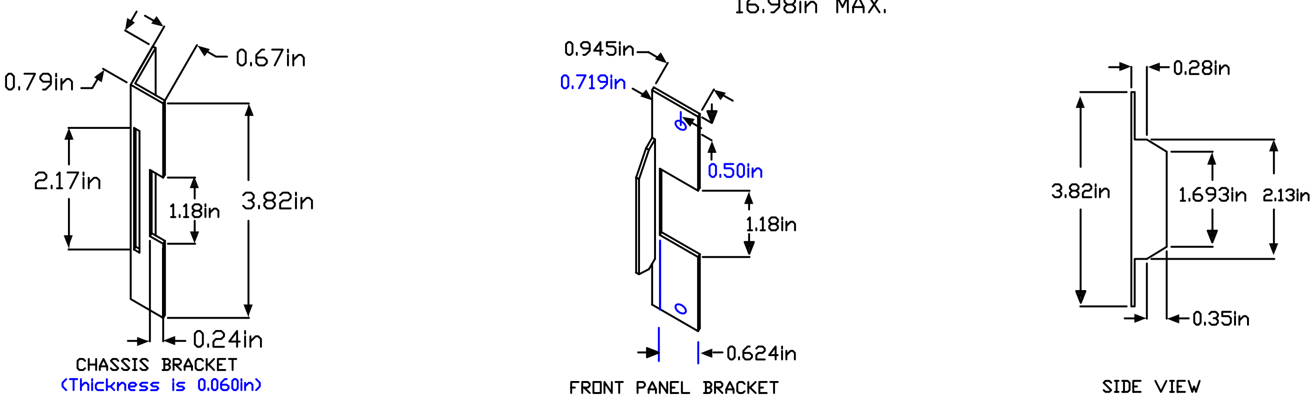
4. The VME Cage Assembly Openning shall be delivered covered by a blank panel. Matching M3 PEM fasteners shall be provided on the back plane surface for panel mounting.

5. Blank plates shall cover all unused module openings.

6. All Module Front Plates thickness shall be (0.08±0.005)

TITLE: MODEL 2070-CHASSIS REAR VIEW	
NO SCALE	A9-2
TEES 2008	





FRONT PANEL ASSEMBLY LATCH DETAILS

NOTES (THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided.

2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 0.51 inch from the Backplane outside surface.

3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.

4. All harnesses shall have a minimum slack of 1 inch when connected.

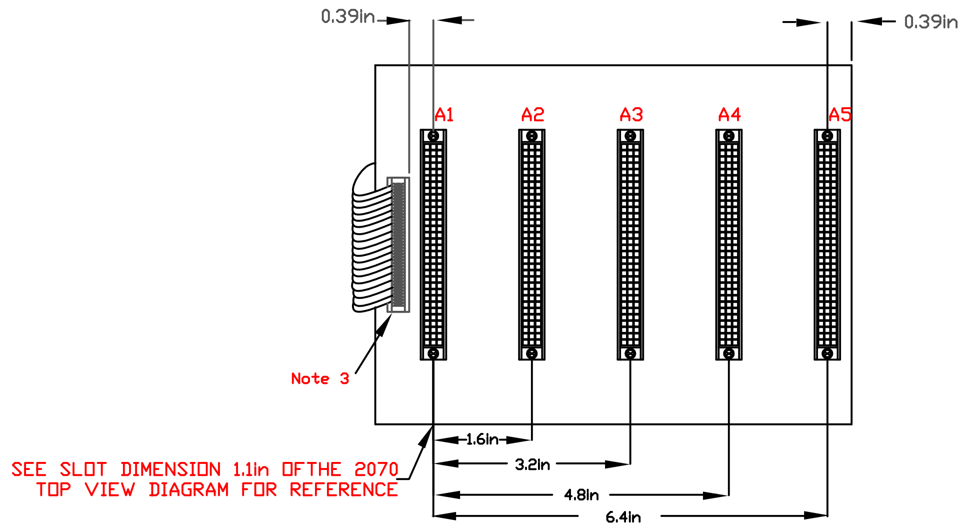
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 0.25 inch above unit baseline.

6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.

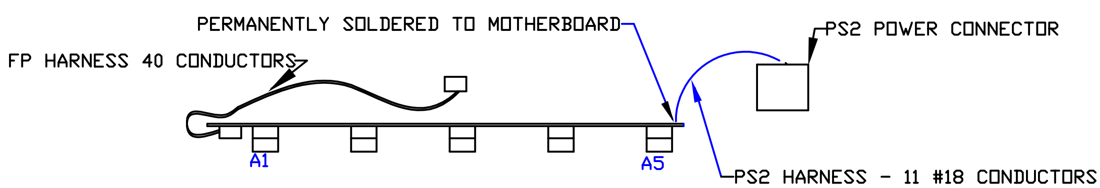
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 0.571 inch folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed 0.71 inch as measured from the front surface of the front panel.

8. Chassis side plates shall be 0.090in thick.

TITLE: MODEL 2070-CHASSIS TOP VIEW	
NO SCALE	A9-3
TEES 2008	



CONNECTOR VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4TXD+	2	SP4TXD-
3	SP4RXD+	4	SP4RXD-
5	SP6TXD+	6	SP6TXD-
7	SP6RXD+	8	SP6RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DCG #1	22	DCG #1
23	+12 VDC SER	24	-12 VDC SER
25	DCG #1	26	DCG #1
27	CPU LED	28	DCG #1
29	CPURESET	30	DCG #1
31	DCG #1	32	C50 ENABLE
33	DCG #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISO +12 VDC
7	DCG #2 (ISO +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

NOTES (THIS DETAIL)

1. The Motherboard shall be a 0.125 inch minimum thickness pcb mechanically mounted in a vertical position.

2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).

3. The FP Harness shall be connected to the motherboard via a header connector. Pin 1 shall be in the lower right hand corner.

4. Front Panel Harness Connector shall intermate with AMP 102-160-9 or equal located on Front Panel PCB.

TITLE: MODEL 2070 CHASSIS MOTHERBOARD	
NO SCALE	A9-4
TEES 2008	

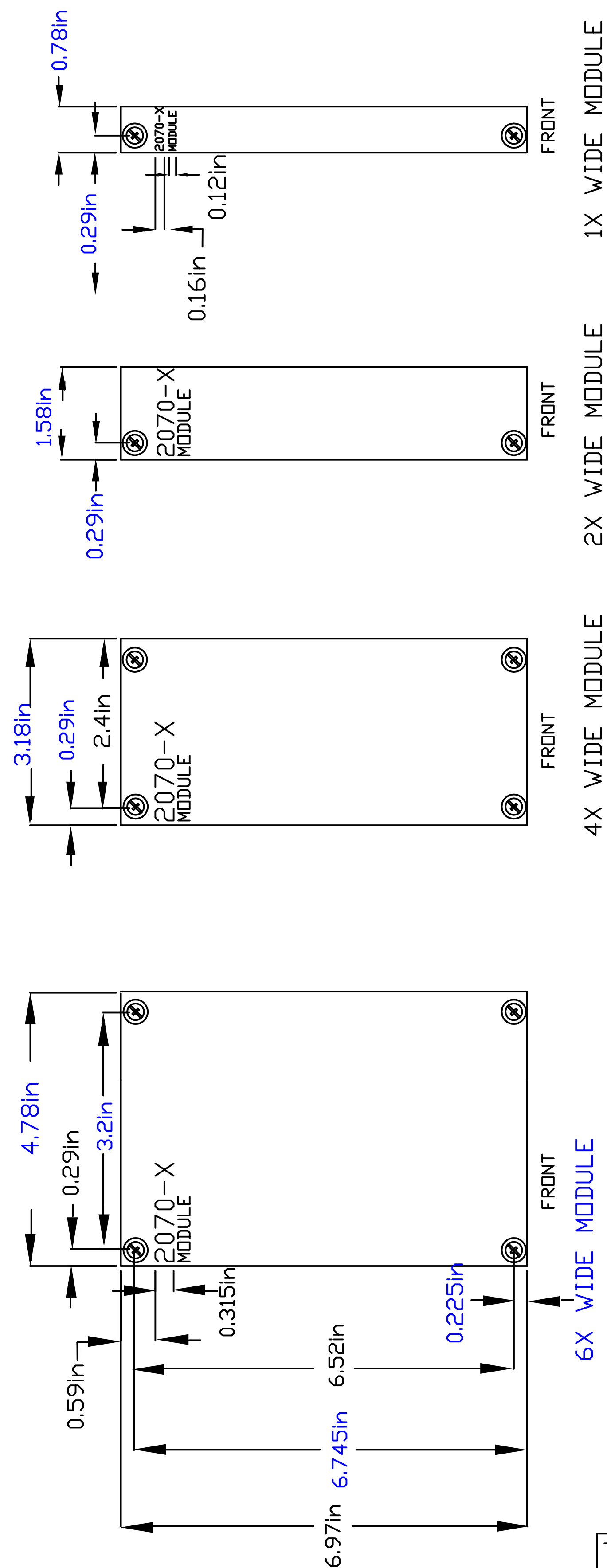
A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXCO+	SP5RXD+
6	SP3RTS-	SP3TXCO-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXCO+
20	NA	NA	SP3TXCO-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NetP5 (TX+)	NA	SP3TXCI-
23	NetP5 (TX-)	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NetP5 (RX+)	POWERUP	CPURESET
26	NetP5 (RX-)	POWERDOWN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

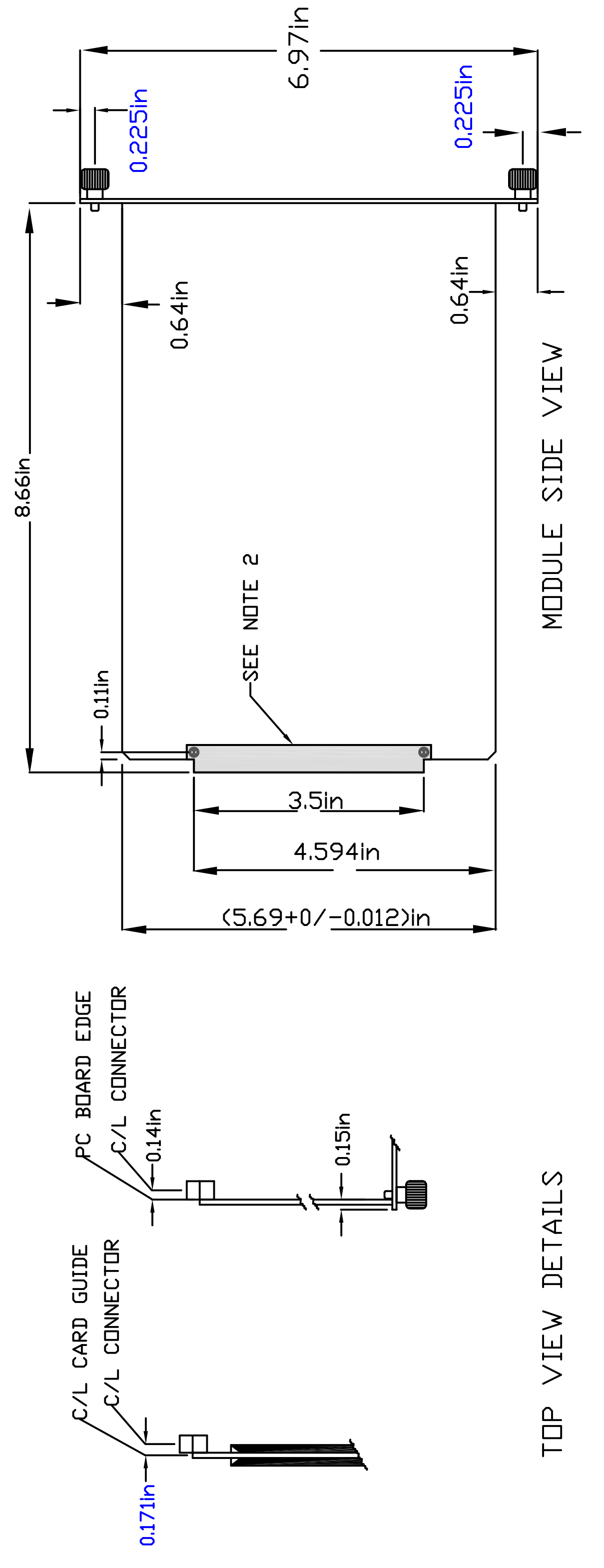
A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXCO+	SP3CTS+
16	SP2RTS-	SP2TXCO-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXCO+
20	SP2DCD-	SP2RXC-	SP3TXCO-
21	DCG #1	NA	SP3TXCI+
22	NetP5 (TX+)	NA	SP3TXCI-
23	NetP5 (TX-)	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NetP5 (RX+)	POWERUP	CPURESET
26	NetP5 (RX-)	POWERDOWN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

NOTES (THIS DETAIL)

1. Functions are referenced to the CPU.
2. DCG #1 for +5VDC and ±12VDC SER.
   DCG #2 for ISO +12 VDC.
3. A1 Connector is the furthest A Connector to the left when viewed from the unit back.
4. Connector A2 to A4, pins B21 and B22 shall read "NA".
   Connector A2, pins B23 shall read "A2 Installed".
   Connector A3, pins B23 shall read "A3 Installed".
   Connector A4, pins B23 shall read "NA".
   Connector A5, pins B21 shall read "A2 Installed".
   Connector A5, pins B22 shall read "DCG #1".
   Connector A5, pins B23 shall read "A3 Installed".
5. Pin A24 (NA) is reserved for network protection only, ie., "Ethernet Shield".
6. Module installed in slot A2 enables SP1 & SP2 on 2070-1x modules.
7. Module installed in slot A3 enables SP5, on 2070-1x modules.
8. SP3 and SP6 are always enabled.
9. "C50 ENABLE" Active (e.g. DCG #1) is used by module installed in slot A1 to disable its channel 2 (i.e. SP4).
10. NetP5 signals TX+, TX-, RX+, RX- respectively.

TITLE: MODEL 2070-MOTHERBOARD A1-A5 CONNECTOR PIN OUT	
NO SCALE	A9-5
TEES 2008	





NOTES (THIS DETAIL)

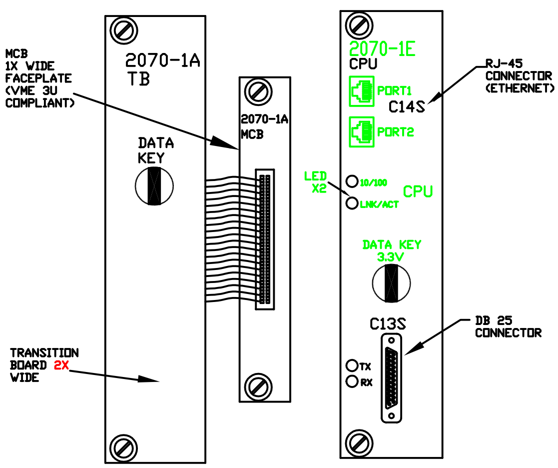
1. All Thumbscrew devices on modules described in this drawing shall be TSD#3 OR EQUAL.

2. 96 pin DIN connector ELCO # 00 8272 96 000 013 OR EQUAL.

TITLE: MODEL 2070-SYSTEM PCB MODULES GENERAL	
NO SCALE	A9-6
TEES 2008	

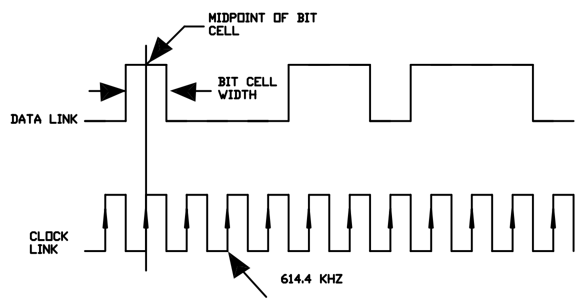
SERIAL PORT REQUIREMENTS			
LOGICAL PORT		RATE KBITS	PROTOCOL
SP1		1.2, NOTE 1	ASYNC
SP1S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP2		1.2, NOTE 1	ASYNC
SP2S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP3		1.2, NOTE 1	ASYNC
SP3S		614.4, NOTE 3	SYNC, HDLC, SDLC
SP4		9.6, NOTE 1	ASYNC
SP5		1.2, NOTE 1	ASYNC
SP5S		614.4	SYNC, HDLC, SDLC
SP6		38.4, NOTE 1	ASYNC
SP8**	NOTE 4	9.6, NOTE 1	ASYNC
SP8S**	NOTE 4	153.6 NOTE 3	SYNC, HDLC, SDLC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



FRONT VIEW FRONT VIEW

CPU FACE PANELS



SDLC TIMING

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8TXD+	14	SP8TXD-
2	SP8RXD+	15	SP8RXD-
3	SP8TXC+	16	SP8TXC-
4	SP8RXC+	17	SP8RXC-
5	SP8RTS+	18	SP8RTS-
6	SP8CTS+	19	SP8CTS-
7	SP8DCD+	20	SP8DCD-
8	NA	21	NA
9	LINESYNC+	22	LINESYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

C14S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES (THIS DETAIL)

1. Additional rates 1.2, 2.4, 4.8, 9.6, 19.2, 38.4.

2. Additional descriptors for other rates:
SPxSa = 19.2, SPxSb = 38.4, SPxSc = 57.6
SPxSd = 76.8, SPxSg = 64.0, SPxSe = 153.6.

3. Additional descriptors for other rates:
SPxSe = 153.6, SPxSf = 614.4.

4. On 2070-1A, SP1 is assigned to 68360 SCC1.
On 2070-1B, SP1 and SP8 are assigned to the dual SCC, and ETHERNET is assigned to 68EN360 SCC1.

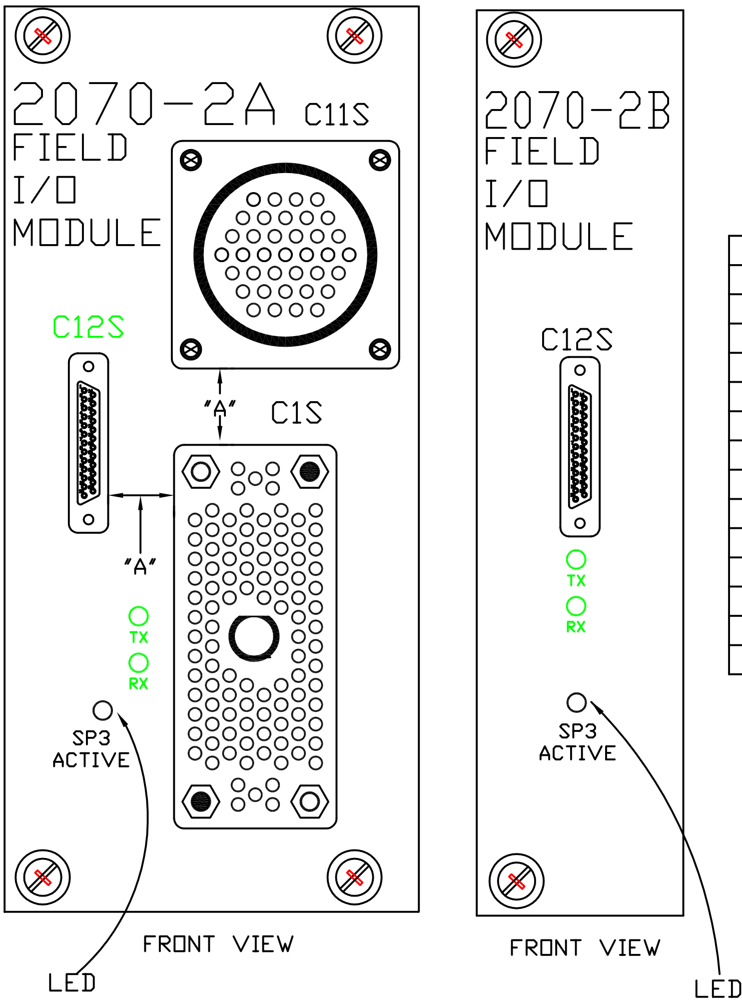
5. A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.

6. BIAS +5VDC (50mA maximum) refers to voltage required for a Line Terminator device and is derived from the ISO +12VDC Power Supply.

7. EG (Equipment Ground) pin is electrically connected to the faceplate.

** 2070-1E only.

TITLE: MODEL 2070-1E CPU MODULES AND SERIAL PORT/SDLC PROTOCOL	
NO SCALE	A9-7
TEES 2008	



FIELD I/O FACE PANELS

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP5TXD+	14	SP5TXD-
2	SP5RXD+	15	SP5RXD-
3	SP5TXC+	16	SP5TXC-
4	SP5RXC+	17	SP5RXC-
5	SP3TXD+	18	SP3TXD-
6	SP3RXD+	19	SP3RXD-
7	SP3TXC+	20	SP3TXC-
8	SP3RXC+	21	SP3RXC-
9	LINE SYNC+	22	LINE SYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

NOTES (THIS DETAIL)

1. 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)

2. Dark Circles in the C1S Connector denote guide pin locations and opencircles denote guide socket locations.

3. Dimension "A" shall be a minimum of 0.5in.

4. C1S - M104 Type. C11S - 37-Pin Circular Plastic Type. C12S - 25-Pin DB Socket Type

5. C12S pin 12 (BIAS +5VDC) at 50mA maximum is derived from the ISO +12 VDC Power Supply. BIAS +5VDC refers to voltage required for a Line Terminator device.

6. EG (Equipment Ground) pin is electrically connected to the faceplate.

7. LED indicators Tx & Rx for SP3 shall be provided (field side).

TITLE: MODEL 2070-2 FIELD I/O MODULES	
NO SCALE	A9-8
TEES 2008	

C1S PIN ASSIGNMENT

PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME
1	DCG #2	27	O24	53	I14	79	I44
2	O0	28	O25	54	I15	80	I45
3	O1	29	O26	55	I16	81	I46
4	O2	30	O27	56	I17	82	I47
5	O3	31	O28	57	I18	83	O40
6	O4	32	O29	58	I19	84	O41
7	O5	33	O30	59	I20	85	O42
8	O6	34	O31	60	I21	86	O43
9	O7	35	O32	61	I22	87	O44
10	O8	36	O33	62	I23	88	O45
11	O9	37	O34	63	I28	89	O46
12	O10	38	O35	64	I29	90	O47
13	O11	39	I0	65	I30	91	O48
14	DCG #2	40	I1	66	I31	92	DCG #2
15	O12	41	I2	67	I32	93	O49
16	O13	42	I3	68	I33	94	O50
17	O14	43	I4	69	I34	95	O51
18	O15	44	I5	70	I35	96	O52
19	O16	45	I6	71	I36	97	O53
20	O17	46	I7	72	I37	98	O54
21	O18	47	I8	73	I38	99	O55
22	O19	48	I9	74	I39	100	O36
23	O20	49	I10	75	I40	101	O37
24	O21	50	I11	76	I41	102	O38 DET RES
25	O22	51	I12	77	I42	103	O39 WDT
26	O23	52	I13	78	I43	104	DCG #2

C11S PIN ASSIGNMENT

PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME
1	O56	11	I25	21	I54	31	DCG #2
2	O57	12	I26	22	I55	32	NA
3	O58	13	I27	23	I56	33	NA
4	O59	14	DCG #2	24	I57	34	NA
5	O60	15	I48	25	I58	35	NA
6	O61	16	I49	26	I59	36	NA
7	O62	17	I50	27	I60	37	DCG #2
8	O63	18	I51	28	I61		
9	DCG #2	19	I52	29	I62		
10	I24	20	I53	30	I63		

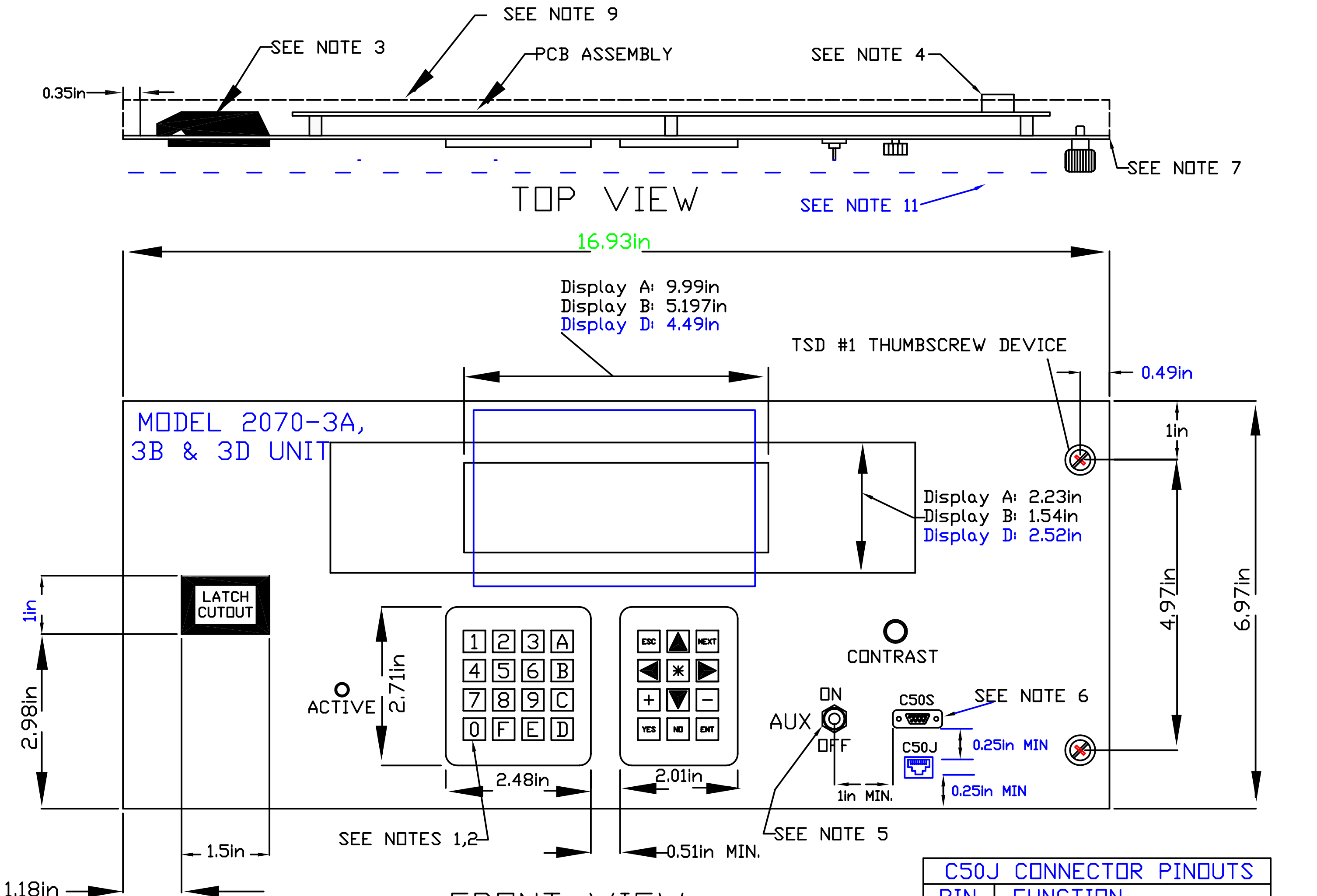
TITLE:

MODEL 2070-2A
FIELD I/O MODULE
C1S & C11S CONNECTORS

NO SCALE

TEES 2008

A9-9



FRONT VIEW

NOTES (THIS DETAIL)

1. Key size shall be (0.3x0.3)in.
2. Key center to center spacing shall be 0.5in.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. The 40 contact connector shall be similar to AMP 102160-9 or equal & compatible to the FP harness in type and pin assignments. Center of the FP harness connector shall be vertically positioned (3.54+/-0.197)in as measured fromthe top of the FPA. The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
5. Two position LOGIC switch mounted vertically.
6. "C50S" connector shall be a DE-9 socket contact connector. "C50J" shall be a RJ-45 8-position jack. "C60P" connector shall be a DE-9 plug contact connector.
7. Front panel sheet metal thickness shall be (0.06±0.005) in.
8. All FPA devices shall be located as shown.
9. The FPA shall be provided with a continuous top and bottom 0.63in (inside dimension) lip bent 90 degrees to the front plate and shall extend the full length of the FPA.
10. C60P B Box Power is +5VDC, 350mA max. All signals on C60 P are referenced to isolated interface ground DCG#3.
11. Components shall not protrude beyond the height of the thumbscrews when tightened.
12. See 9.4.1 for components required.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4RXD
3	SP4TXD
4	NA
5	DCG #1
6	NA
7	NA
8	NA
9	NA

C50J CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP4RXD
3	C50 ENABLE
4	NA
5	SP4TXD
6	DCG #1
7	NA
8	NA

C60P CONNECTOR PINOUTS	
PIN	FUNCTION
1	B Box Power, Note 10
2	SP6RXD
3	SP6TXD
4	NA
5	DCG #3
6	NA
7	CPURESET
8	NA
9	CPU LED

TITLE: MODEL 2070-3A, 3B & 3D FRONT PANEL ASSEMBLY	
NO SCALE	A9-10
TEES 2008	

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	0D

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
NO SCALE	A9-11
TEES 2008	

CONFIGURATION COMMAND CODES

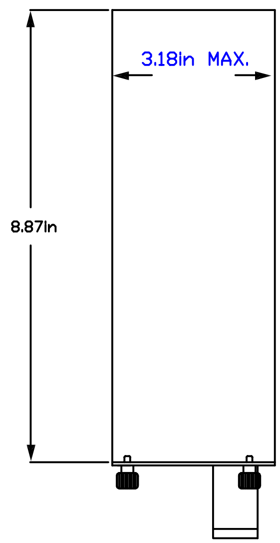
ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py ; Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn ; Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 5B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Pn = 0 : Clear Tab at Current Position, Pn = 3 : Clear All Tabs
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 12 h	1B 5B 3F 31 32 68	Heater on
ESC [? 12 l	1B 5B 3F 31 32 6C	Heater off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTE: 1. Numerical values have one ASCII character per digit without leading zero.
2. Reverse Video & Underline NOT required for Front Panel Assembly Option 3A 3B & 3D.
Command codes shall be available for Option 3C (C60P).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Py; Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B....P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)
ESC [h n	1B 5B 68 6E	ESC [P1 R	1B 5B P1 52	P1: Heater (h,l)
ESC [c	1B 5B 63	ESC [P1 R	1B 5B P1 52	P1; Type (A,B,D)

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY DISPLAY KEY CODES	
NO SCALE	A9-12
TEES 2008	



TOP VIEW

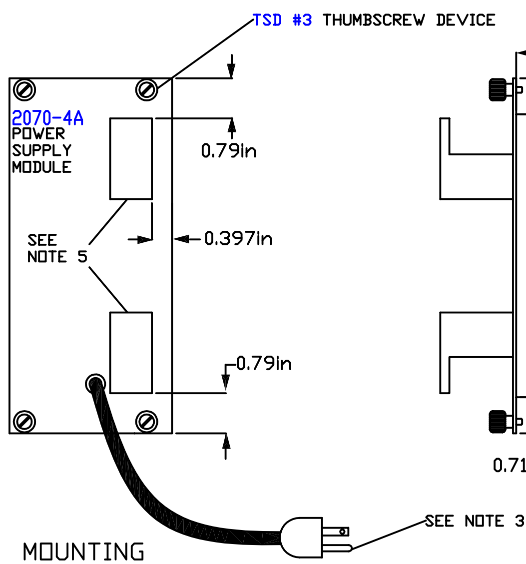
PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	+5 VDC SENSE
7	DCG #1 SENSE
8	AC FAIL
9	SYSRESET
10	NA

PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISO +12 VDC
7	DCG #2 (ISO +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

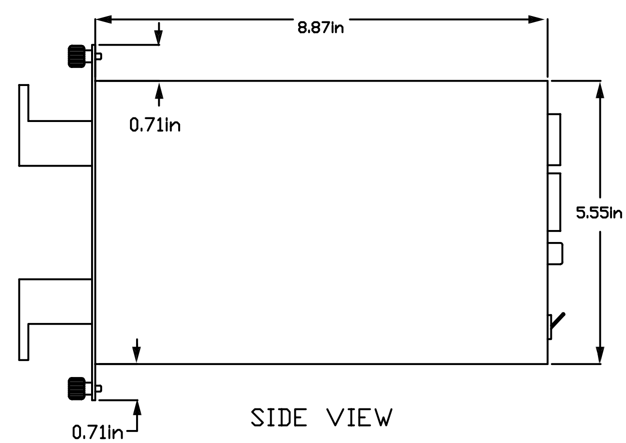
NOTES (THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three #16 conductor power cable, 40 inch minimum length and permanenlty attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row MATE-N-LOK CAP Connectors with locking latch devices (OR EQUAL).

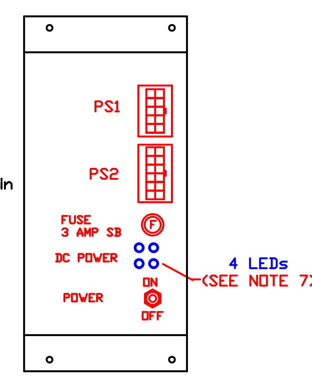
   PS1 connector shall be a 10 position PLUG connector.
   PS2 connector shall be a 12 position PLUG connector.
5. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, ISO +12, +12 SER, -12 SER).
8. Power Supply shall be marked as 2070-4A.



MOUNTING
PLATE
REAR VIEW



SIDE VIEW



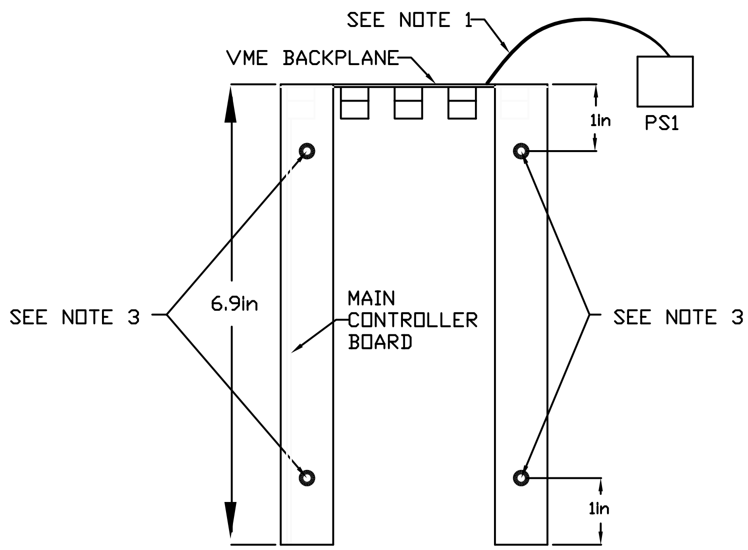
FRONT VIEW

TITLE:
MODEL 2070-4
POWER SUPPLY MODULE

NO SCALE

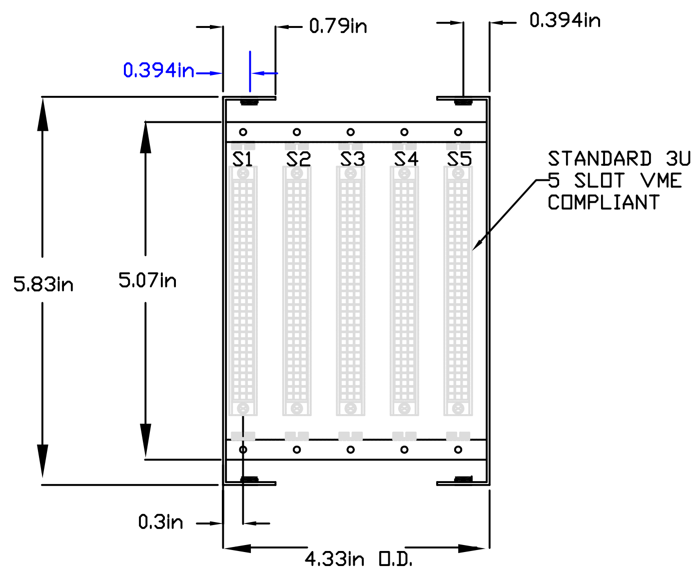
TEES 2008

A9-13



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & ±12 SER)
5	+5 VDC Standby
6	+5 VDC SENSE
7	DCG #1 SENSE
8	AC FAIL
9	SYSRESET
10	NA



FRONT VIEW

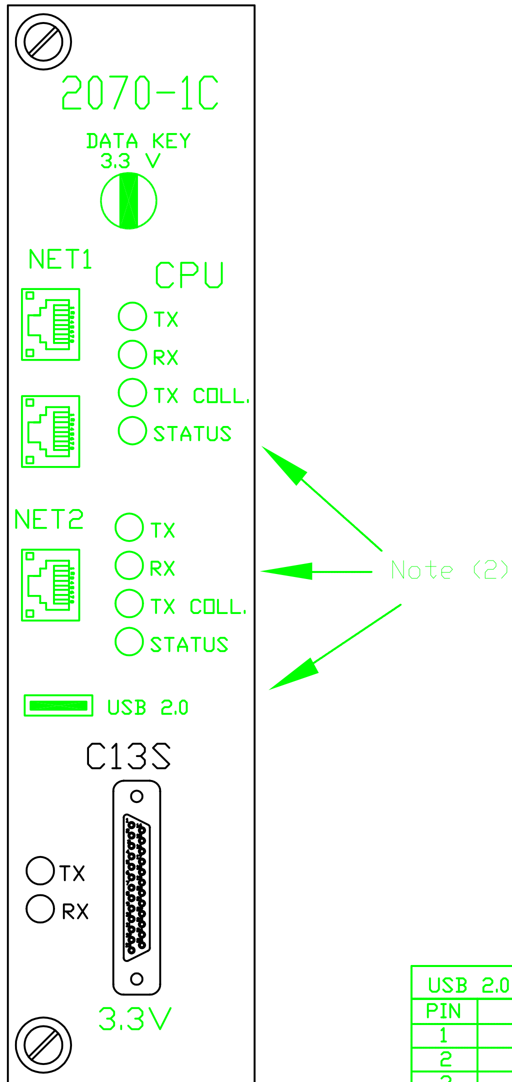
NOTES (THIS DETAIL)

1. PS1 Harness interfaces between the Model 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, FastOn or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.

2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via TSD #3 thumbscrews. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.

3. 6-32 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.

TITLE: MODEL 2070-5 VME CAGE ASSEMBLY	
NO SCALE	A9-14
TEES 2008	



USB 2.0 PIN ASSIGNMENT	
PIN	FUNCTION
1	VCC
2	DATA-
3	DATA+
4	GND

NET1 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NET2 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

NOTES: (THIS DETAIL)

1. BIAS +5VDC refers to voltage required for a Line Terminator device.
2. NET1, NET2, USB & C13S should be placed within the area as shown.

TITLE:

MODEL 2070-1C CPU

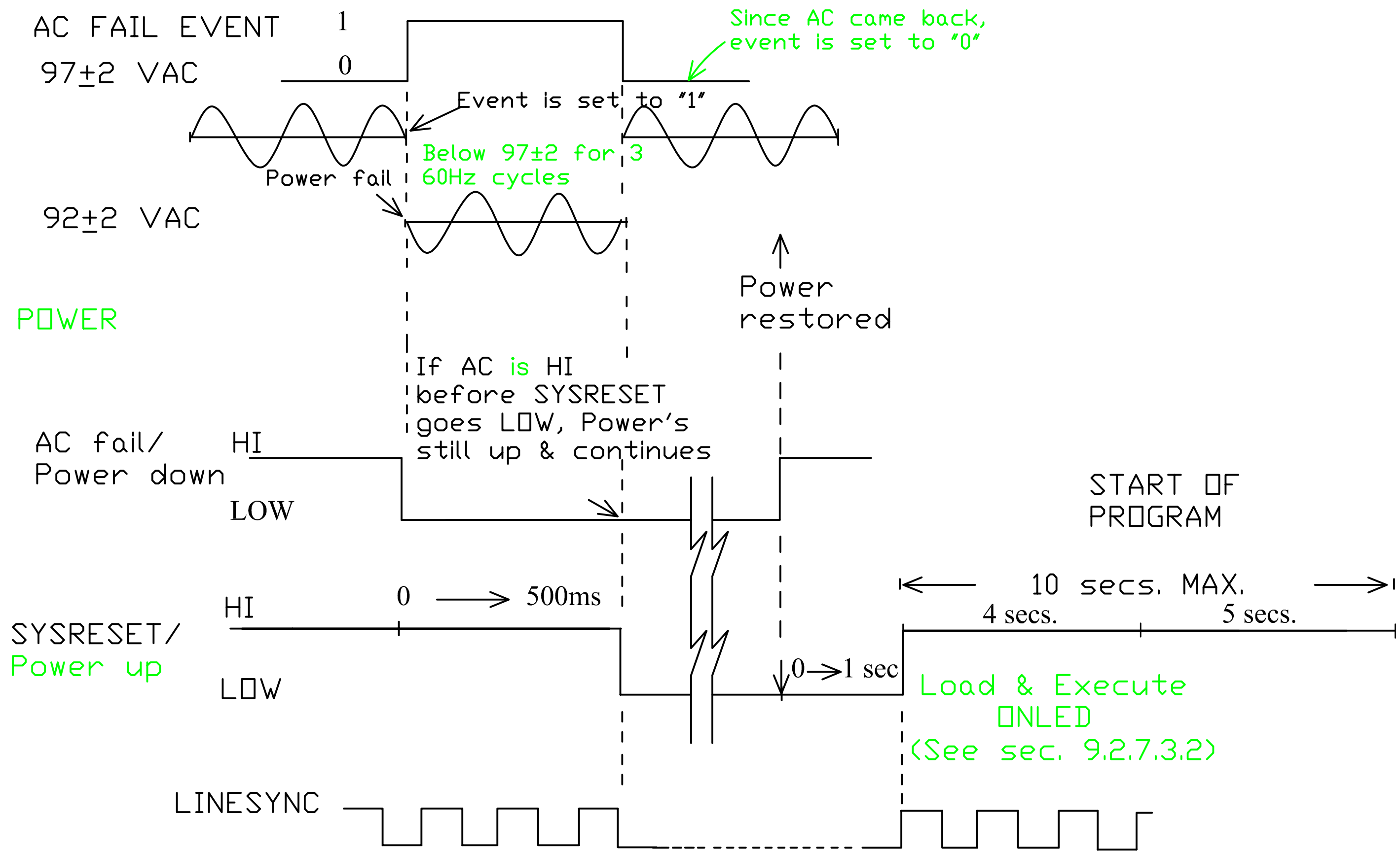
NO SCALE

TEES 2008

A9-15

CONNECTOR P1	CONNECTOR P2
1 RESERVED	1 RESERVED
2 RESERVED	2 STANDBY +3.3 Volts
3 RESERVED	3 VPRIMARY + 3.3 Volts
4 RESERVED	4 VPRIMARY + 3.3 Volts
5 GROUND	5 SP2 TXD
6 GROUND	6 SP2 RXD
7 GROUND	7 SP2 RTS
8 GROUND	8 SP2 CTS
9 SP1 TXD	9 SP2 CD
10 SP1 RXD	10 SP2 TXC INT
11 SP1 RTS	11 SP2 TXC EXT
12 SP1 CTS	12 SP2 RXC EXT
13 SP1 CD	13 SP5 TXD
14 SP1 TXC INT	14 SP5 RXD
15 SP1 TXC EXT	15 SP5 TXC
16 SP1 RXC EXT	16 SP5 RXC
17 SP3 TXD	17 USB POWER SWITCH
18 SP3 RXD	18 USB OVER CURRENT
19 SP3 RTS	19 USB DATA+
20 SP3 CTS	20 USB DATA-
21 SP3 CD	21 SP8 TXD
22 SP3 TXC INT	22 SP8 RXD
23 SP3 TXC EXT	23 SP8 RTS
24 SP3 RXC EXT	24 SP8 CTS
25 SP4 TXD	25 SP8 CD
26 SP4 RXD	26 SP8 TXC INT
27 SP6 TXD	27 SP8 RXC EXT
28 SP6 RXD	28 CPU_RESET
29 CPU_ACTIVE LED	29 LINESYNC
30 ENET 1 TXD+	30 POWERDOWN
31 ENET 1 TXD-	31 POWERUP
32 ENET 1 RXD+	32 SPI MOSI
33 ENET 1 RXD-	33 SPI MISO
34 ENET 1 COL LED	34 SPI CLK
35 ENET 1 DUP LED	35 SPI SELECT 1
36 ENET 1 SPD LED	36 SPI SELECT 2
37 ENET 1 LNK LED	37 SPI SELECT 3
38 ENGINE PRESENT	38 SPI SELECT 4
39 ENET 2 TXD+	39 DATA_KEY PRESENT
40 ENET 2 TXD-	40 PROG TEST
41 ENET 2 RXD+	41 PROG TEST
42 ENET 2 RXD-	42 PROG TEST
43 ENET 2 COL LED	43 PROG TEST
44 ENET 2 DUP LED	44 PROG TEST
45 ENET 2 SPD LED	45 PROG TEST
46 ENET 2 LNK LED	46 PROG TEST
47 ENET 1 BaseT Sense	47 PROG TEST
48 ENET 2 BaseT Sense	48 PROG TEST
49 RESERVED	49 PROG TEST
50 RESERVED	50 PROG TEST

TITLE: ENGINE BOARD P1 & P2 CONNECTOR PIN ASSIGNMENTS	
NO SCALE	A9-16
TEES 2008	



Note:

Power Failure: A Power Failure is said to have occured when the incoming line voltage falls below 92+/-2 VAC for 50ms. See Power Conditions.

Power Restoration: Power is said to be restored when the incoming line voltage equals or exceeds 97+/-2 VAC for 50ms. See Power Conditions.

Power Conditions: A 16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (60 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.

TITLE:

MODEL 2070
POWER FAILURE REACTION

NO SCALE

TEES 2008

A9-17

APPENDIX A10
CHAPTER DETAILS

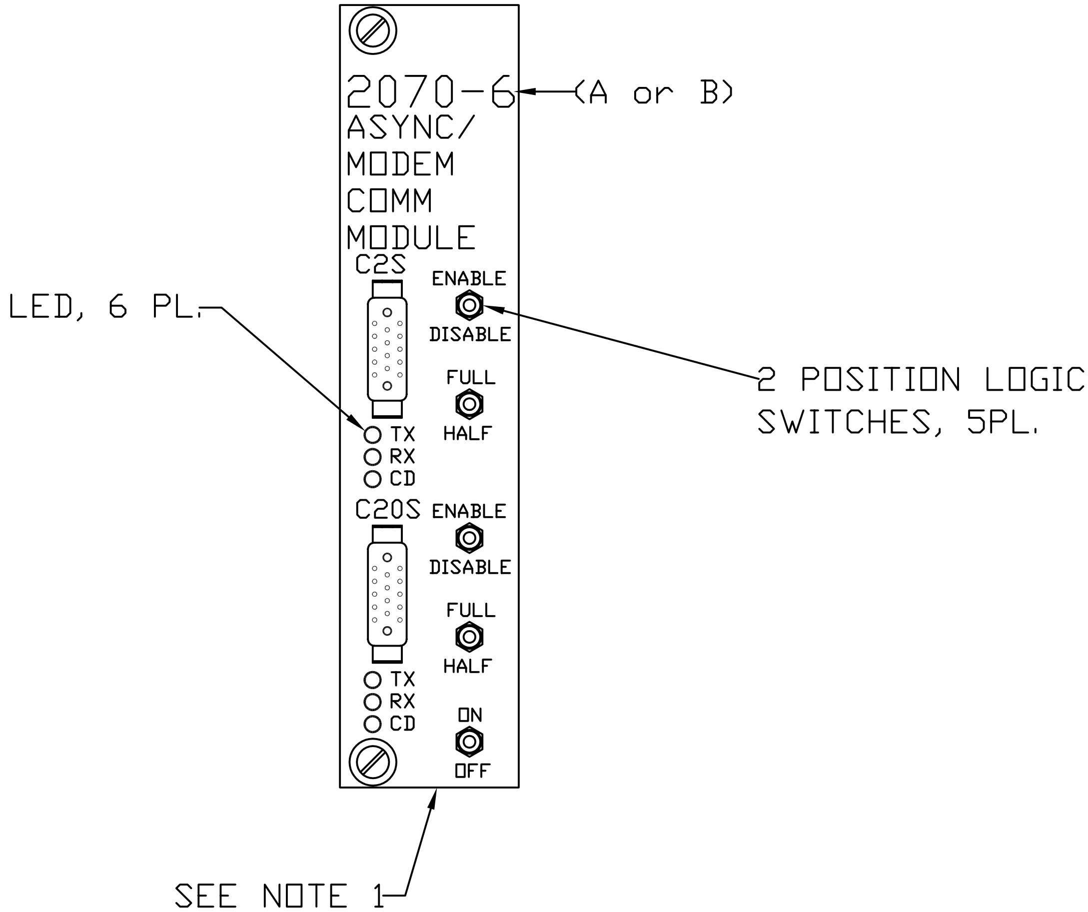
GENERAL NOTES

The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on the module.

Line drivers/receivers shall be socket or surface mounted.

Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.

The Comm modules shall be "Hot" swappable without damage to circuitry or operations.



C2S & C20S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	RXD
C	AUDIO OUT	L	TXD
D	IFC +5 VDC	M	CTS
E	AUDIO OUT	N	IFC GND
F	NA	P	NA
H	DCD	R	NA

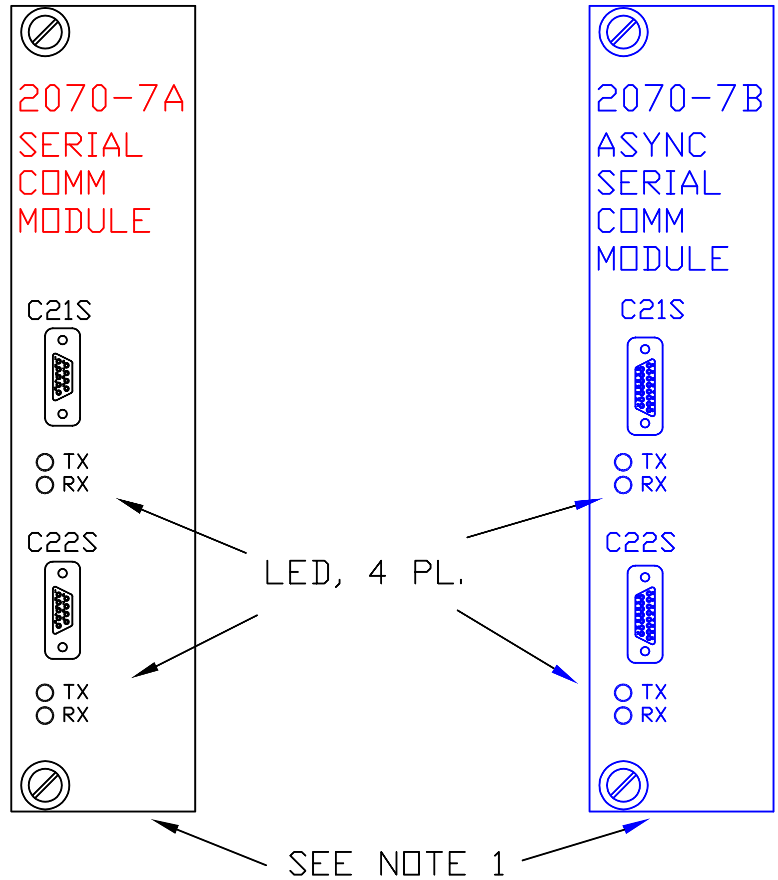
NOTES (THIS DETAIL)

1. 2X Faceplate
(See 2070 System
PCB Module, Detail A9-6).

2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

3. IFC (Interface) Power and Ground is isolated from the internal ground system & is the voltage reference for the EIA-232 signals also.

TITLE: MODEL 2070-6A, 6B ASYNC/MODEM SERIAL COMMUNICATION MODULE	
NO SCALE	A10-1
TEES 2008	



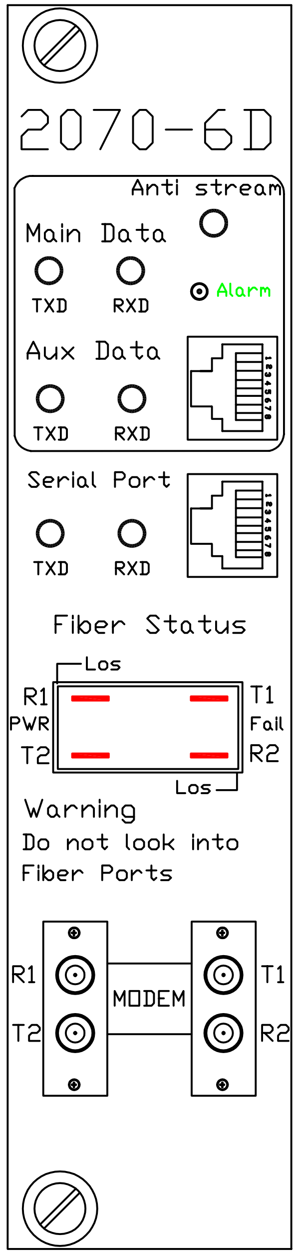
2070-7A (DE-9S)	
C21S & C22S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

2070-7B (DA-15S)			
C21S & C22S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TXD+	9	TXD-
2	IFC GND	10	IFC GND
3	TXC+	11	TXC-
4	IFC GND	12	IFC GND
5	RXD+	13	RXD-
6	IFC GND	14	IFC GND
7	RXC+	15	RXC-
8	NA		

NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. Connectors 21 & 22 are DE 9S for Module 7A & DA 15S for Module 7B.
3. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.
4. On 2070-7B, SPxRTS shall enable/disable TXD+/- & TXCO+/-
5. TXC is jumper selectable to be either TXCO or TXCI.

TITLE: MODEL 2070-7A, 7B ASYNC/SYNC SERIAL COMMUNICATION MODULE	
NO SCALE	A10-2
TEES 2008	



AUX. PORT PIN OUT ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	N/C	5	RXD
2	DCD/KOD	6	TXD
3	N/C	7	CTS
4	GND	8	RTS

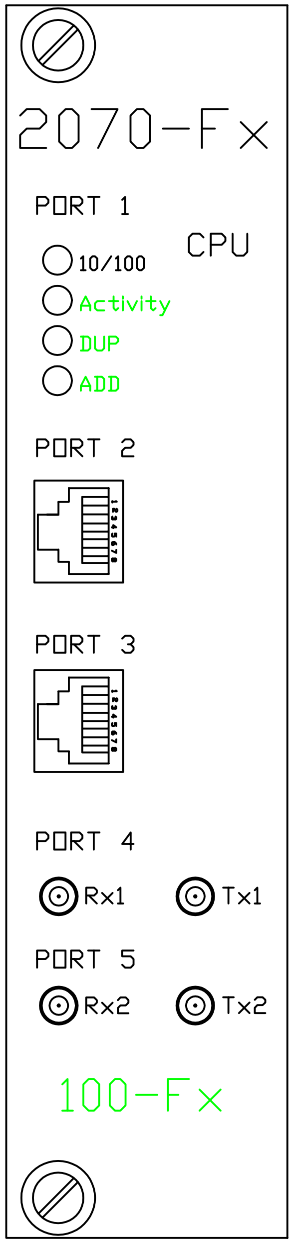
SERIAL PORT PIN OUT ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	+5 VDC	5	RXD
2	DCD	6	TXD
3	N/C	7	CTS
4	GND	8	RTS

TITLE: MODEL 2070 6D
FIBER OPTICS MODEM
COMMUNICATION MODULE

NO SCALE

TEES 2008

A10-3



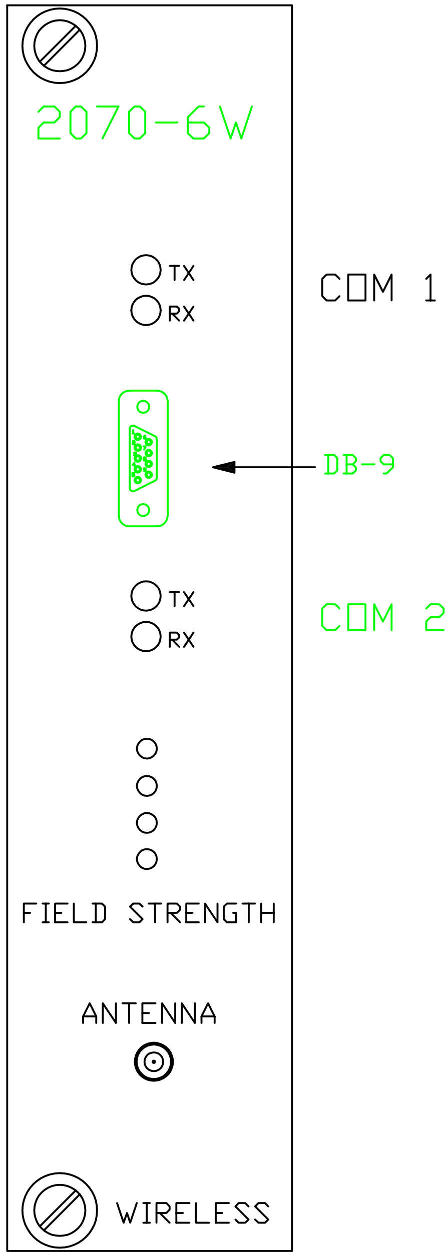
PORT 2 & 3 RJ45 PIN ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX −	6	RX −
3	RX +	7	NA
4	NA	8	NA

TITLE: MODEL 2070-Fx FIBER OPTICS NETWORK COMMUNICATION MODULE

NO SCALE

TEES 2008

A10-4



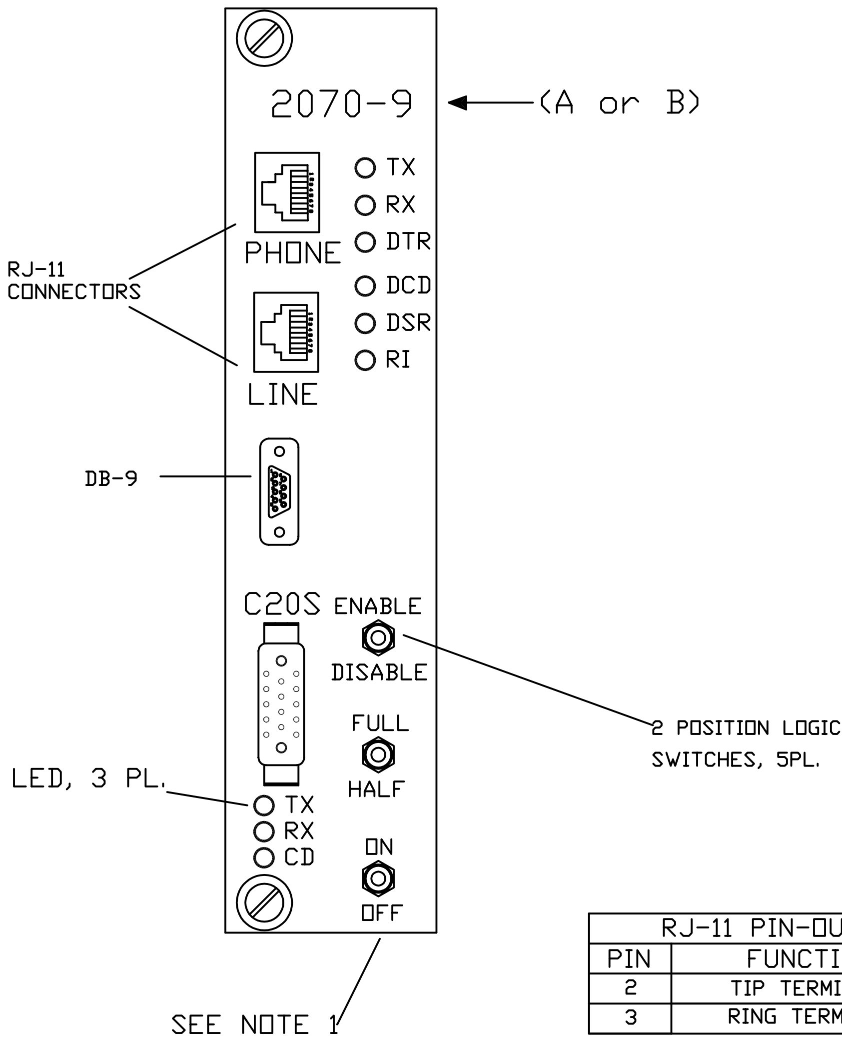
2070-9W (DB-9) C21S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).

2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.

TITLE: MODEL 2070-6W WIRELESS MODEM COMMUNICATION MODULE	
NO SCALE	A10-5
TEES 2008	



RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

C20S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	RXD
C	AUDIO OUT	L	TXD
D	IFC +5 VDC	M	CTS
E	AUDIO OUT	N	IFC GND
F	NA	P	NA
H	DCD	R	NA

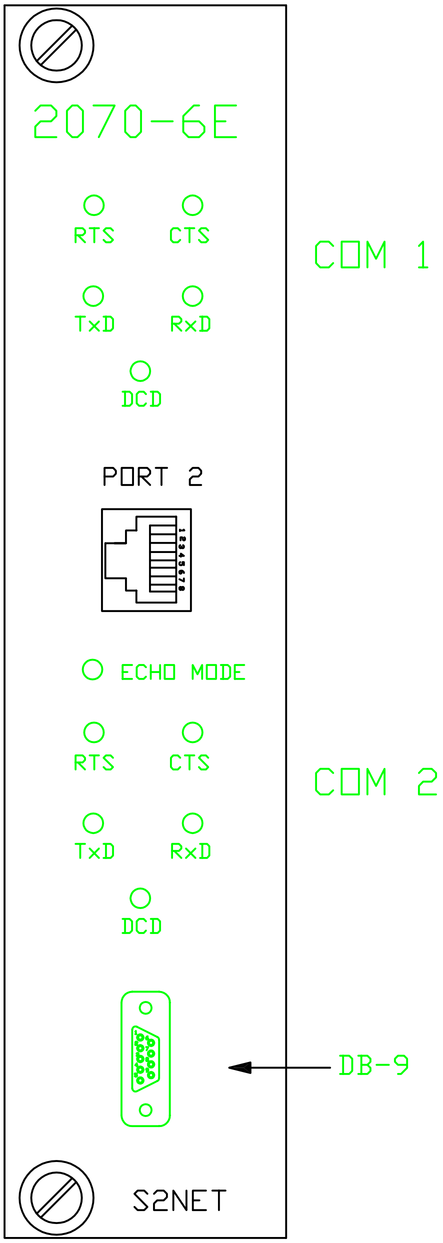
NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).

2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.

3. IFC (Interface) Power and Ground is isolated from the internal ground system & is the voltage reference for the EIA-232 signals also.

TITLE: MODEL 2070-9A, 9B FSK/DIAL UP MODEM COMMUNICATION MODULE	
NO SCALE	A10-6
TEES 2008	



DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	DC GND
6	NA
7	RTS
8	CTS
9	NA

RJ45 ETHERNET PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX −	6	NA
3	RX +	7	NA
4	RX−	8	NA

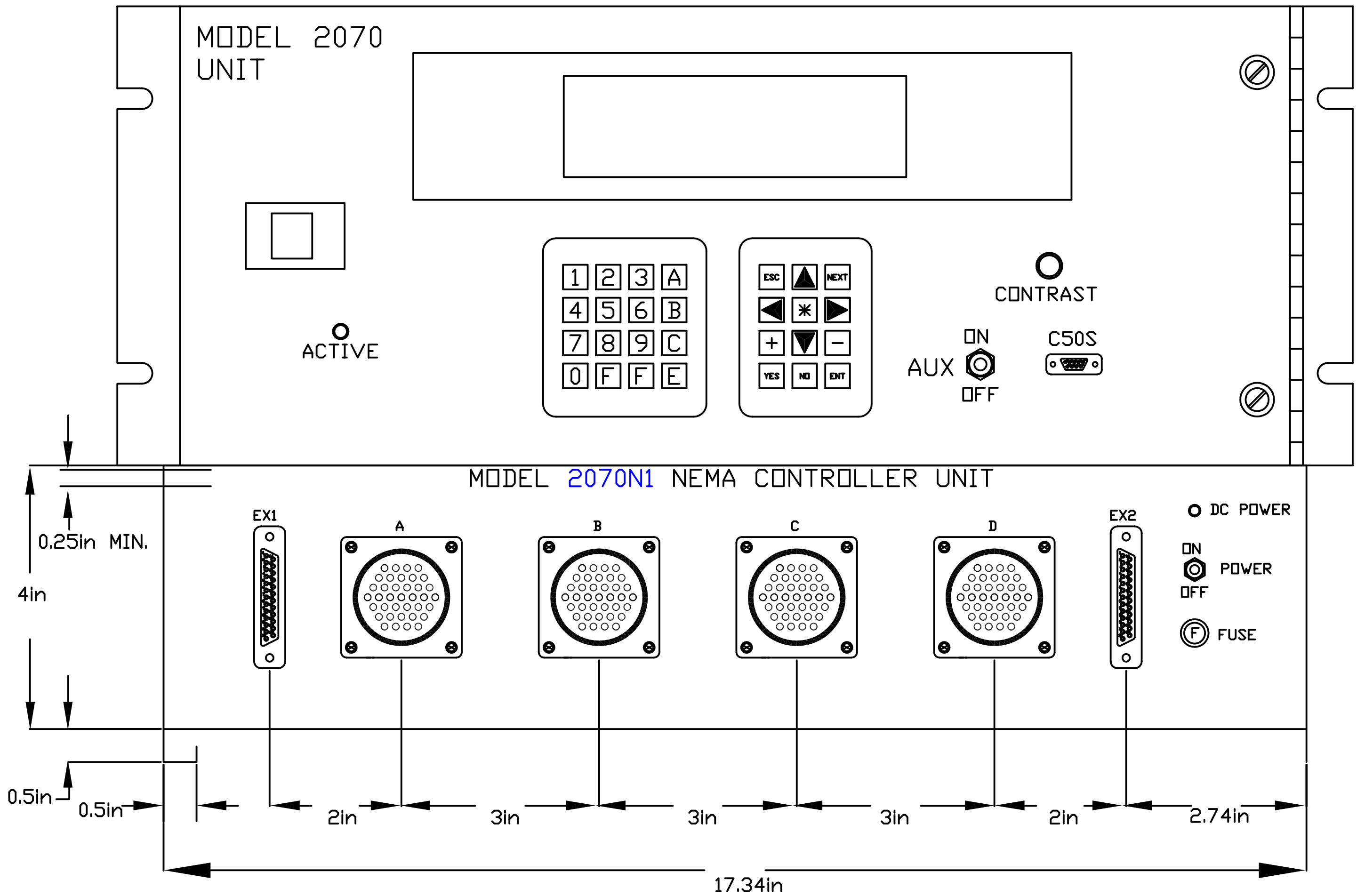
NOTES (THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).

2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.

TITLE: MODEL 2070-6E SERIAL 2 NETWORK COMMUNICATION MODULE	
NO SCALE	A10-7
TEES 2008	

APPENDIX A11
CHAPTER 11 DETAILS



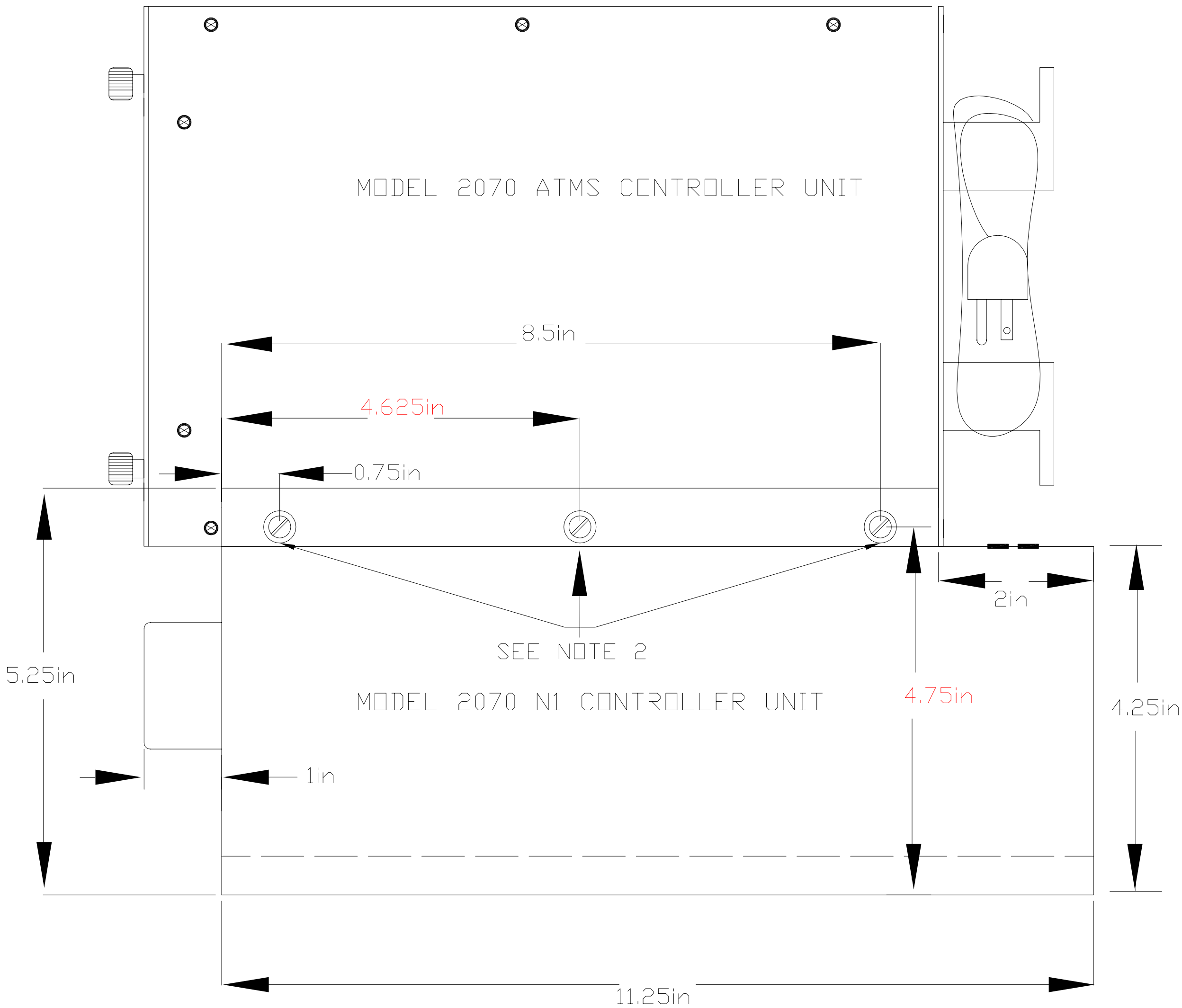
NOTES (THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for refernce.

2. The bottom supports shall be double flanged.

3. A = Connector A (MS-3112-22-55P Type)
   B = Connector B (MS-3112-22-55S Type)
   C = Connector C (MS-3112-24-61S Type)
   D = Connector D (MS-3112-24-61P Type)
   EX1 = Connector EX1 (DB-25S Type)
   EX2 = Connector EX2 (DB-25S Type)

TITLE: 2070 (V or L) N1 CONTROLLER UNIT FRONT VIEW	
NO SCALE	A11-1
TEES 2008	

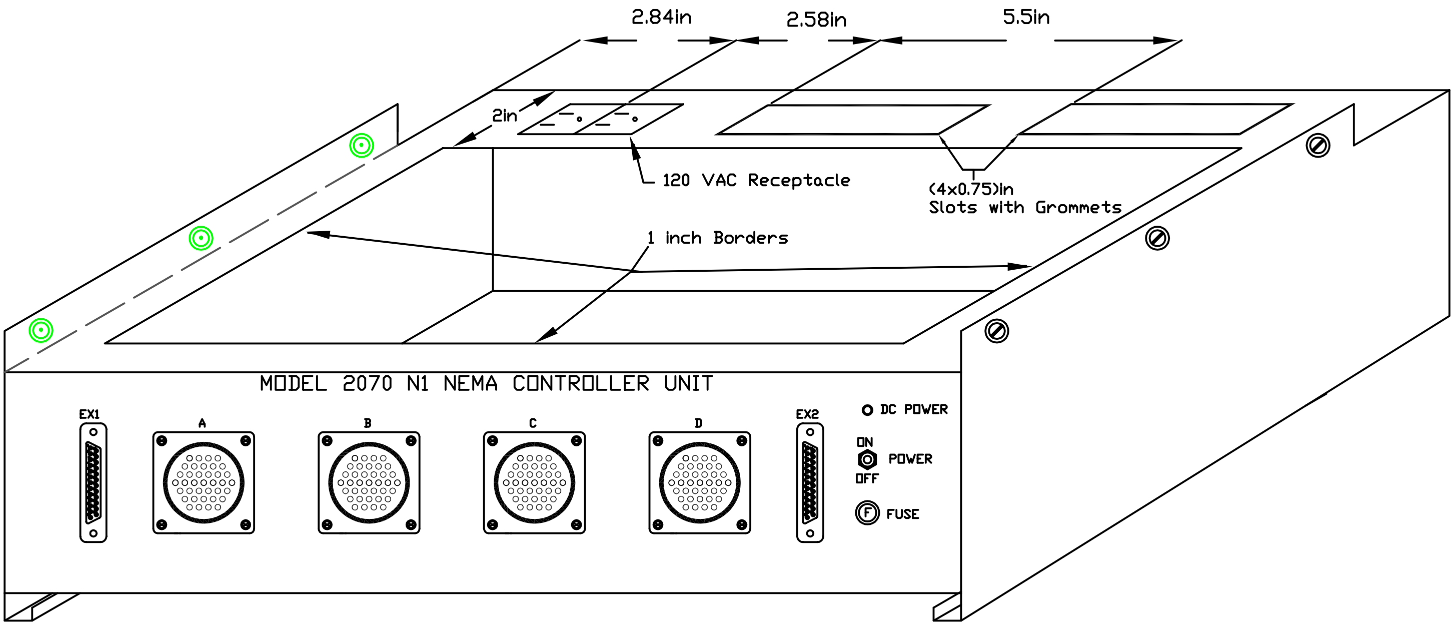


NOTES (THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.

2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module.

TITLE: 2070 (V or L) N1 CONTROLLER UNIT SIDE VIEW	
NO SCALE	A11-2
TEES 2008	



NOTES (THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.

TITLE: 2070 (V or L) N1 CONTROLLER UNIT ISO VIEW	
NO SCALE	A11-3
TEES 2008	

PIN	CONNECTOR A — FUNCTION: NAME	CONNECTOR A — FUNCTION: PORT	CONNECTOR B — FUNCTION: NAME	CONNECTOR B — FUNCTION: PORT
A	Fault Monitor	---	Phase 1 Next	O8-1
B	+24 VDC External	---	Reserved	I9-5
C	Voltage Monitor	---	Phase 2 Next	O8-2
D	Phase 1 Red	O1-1	Phase 3 Green	O3-3
E	Phase 1 Don't Walk	O4-1	Phase 3 Yellow	O2-3
F	Phase 2 Red	O1-2	Phase 3 Red	O1-3
G	Phase 2 Don't Walk	O4-2	Phase 4 Red	O1-4
H	Phase 2 Ped Clear	O5-2	Phase 4 Ped Clear	O5-4
J	Phase 2 Walk	O6-2	Phase 4 Don't Walk	O4-4
K	Phase 2 Vehicle Detector	I1-2	Phase 4 Check	O7-4
L	Phase 2 Pedestrian Detector	I2-2	Phase 4 Vehicle Detector	I1-4
M	Phase 2 Hold	I3-2	Phase 4 Pedestrian Detector	I2-4
N	Stop Timing (Ring 1)	I6-2	Phase 3 Vehicle Detector	I1-3
P	Inh Max Term (Ring 1)	I6-3	Phase 3 Pedestrian Detector	I2-3
R	External Start	I8-1	Phase 3 Omit	I5-3
S	Interval Advance	I8-2	Phase 2 Omit	I5-2
T	Indicator Lamp Control	I8-3	Phase 5 Ped Omit	I4-5
U	AC Neutral	---	Phase 1 Omit	I5-1
V	Chassis Ground	---	Ped Recycle (Ring 2)	I7-5
W	2070N DC Ground	---	Reserved	I9-6
X	Flashing Logic Out	O11-7	Reserved	I9-7
Y	Coded Status Bit C (Ring 1)	O12-3	Phase 3 Walk	O6-3
Z	Phase 1 Yellow	O2-1	Phase 3 Ped Clear	O5-3
a	Phase 1 Ped Clear	O5-1	Phase 3 Don't Walk	O4-3
b	Phase 2 Yellow	O2-2	Phase 4 Green	O3-4
c	Phase 2 Green	O3-2	Phase 4 Yellow	O2-4
d	Phase 2 Check	O7-2	Phase 4 Walk	O6-4
e	Phase 2 On	O9-2	Phase 4 On	O9-4
f	Phase 1 Vehicle Detector	I1-1	Phase 4 Next	O8-4
g	Phase 1 Pedestrian Detector	I2-1	Phase 4 Omit	I5-4
h	Phase 1 Hold	I3-1	Phase 4 Hold	I3-4
i	Force Off (Ring 1)	I6-1	Phase 3 Hold	I3-3
j	Min Recall All Phases	I8-4	Phase 3 Ped Omit	I4-3
k	Manual Control Enable	I8-5	Phase 6 Ped Omit	I4-6
m	Call To Non-Actuated I	I6-8	Phase 7 Ped Omit	I4-7
n	Test Input A	I9-1	Phase 8 Ped Omit	I4-8
p	AC Power	---	Overlap A Yellow	O10-2
q	I/O Mode Bit A	I8-6	Overlap A Red	O10-3
r	Coded Status Bit B (Ring 1)	O12-2	Phase 3 Check	O7-3
s	Phase 1 Green	O3-1	Phase 3 On	O9-3
t	Phase 1 Walk	O6-1	Phase 3 Next	O8-3
u	Phase 1 Check	O7-1	Overlap D Red	O11-6
v	Phase 2 Ped Omit	I4-2	Reserved	I9-8
w	Omit All-Red Clear (Phase 1)	I6-7	Overlap D Green	O11-4
x	Red Rest Mode (Ring 1)	I6-4	Phase 4 Ped Omit	I4-4
y	I/O Mode Bit B	I8-7	Not Assigned	---
z	Call To Non-Actuated II	I7-8	Max II Selection (Ring 2)	I7-6
AA	Test Input B	I9-2	Overlap A Green	O10-1
BB	Walk Rest Modifier	I9-4	Overlap B Yellow	O10-5
CC	Coded Status Bit A (Ring 1)	O12-1	Overlap B Red	O10-6
DD	Phase 1 On	O9-1	Overlap C Red	O11-3
EE	Phase 1 Ped Omit	I4-1	Overlap D Yellow	O11-5
FF	Pedestrian Recycle (Ring 1)	I6-5	Overlap C Green	O11-1
GG	Max II Selection (Ring 1)	I6-6	Overlap B Green	O10-4
HH	I/O Mode Bit C	I8-8	Overlap C Yellow	O11-2

TITLE: 2070-8 FILELD I/O MODULE CONECTOR A & B

NO SCALE

TEES 2008

A11-4

PIN	CONNECTOR C FUNCTION NAME	PORT	CONNECTOR D FUNCTION NAME	PORT
A	Coded Status Bit A (Ring 2)	O12-4	Detector 9	I10-1
B	Coded Status Bit B (Ring 2)	O12-5	Detector 10	I10-2
C	Phase 8 Don't Walk	O4-8	Detector 11	I10-3
D	Phase 8 Red	O1-8	Detector 12	I10-4
E	Phase 7 Yellow	O2-7	Detector 13	I10-5
F	Phase 7 Red	O1-7	Detector 14	I10-6
G	Phase 6 Red	O1-6	Detector 15	I10-7
H	Phase 5 Red	O1-5	Detector 16	I10-8
J	Phase 5 Yellow	O2-5	Detector 17	I11-1
K	Phase 5 Ped Clear	O5-5	Detector 18	I11-2
L	Phase 5 Don't Walk	O4-5	Detector 19	I11-3
M	Phase 5 Next	O8-5	Detector 20	I11-4
N	Phase 5 On	O9-5	Detector 21	I11-5
P	Phase 5 Vehicle Detector	I1-5	Detector 22	I11-6
R	Phase 5 Pedestrian Detector	I2-5	Detector 23	I11-7
S	Phase 6 Vehicle Detector	I1-6	Detector 24	I11-8
T	Phase 6 Pedestrian Detector	I2-6	Clock Update	I12-1
U	Phase 7 Pedestrian Detector	I2-7	Hardware Control	I12-2
V	Phase 7 Vehicle Detector	I1-7	Cycle Advance	I12-3
W	Phase 8 Pedestrian Detector	I2-8	Max 3 Selection	I12-4
X	Phase 8 Hold	I3-8	Max 4 Selection	I12-5
Y	Force Off (Ring 2)	I7-1	Free	I12-6
Z	Stop Timing (Ring 2)	I7-2	Not Assigned	I12-7
a	Inhibit Max Timing (Ring 2)	I7-3	Not Assigned	I12-8
b	Test Input C	I9-3	Alarm 1	I13-1
c	Coded Status Bit C (Ring 2)	O12-6	Alarm 2	I13-2
d	Phase 8 Walk	O6-8	Alarm 3	I13-3
e	Phase 8 Yellow	O2-8	Alarm 4	I13-4
f	Phase 7 Green	O3-7	Alarm 5	I13-5
g	Phase 6 Green	O3-6	Flash In	I13-6
h	Phase 6 Yellow	O2-6	Conflict Monitor Status	I13-7
i	Phase 5 Green	O3-5	Door Ajar	I13-8
j	Phase 5 Walk	O6-5	Special Function 1	I14-1
k	Phase 5 Check	O7-5	Special Function 2	I14-2
m	Phase 5 Hold	I3-5	Special Function 3	I14-3
n	Phase 5 Omit	I5-5	Special Function 4	I14-4
p	Phase 6 Hold	I3-6	Special Function 5	I14-5
q	Phase 6 Omit	I5-6	Special Function 6	I14-6
r	Phase 7 Omit	I5-7	Special Function 7	I14-7
s	Phase 8 Omit	I5-8	Special Function 8	I14-8
t	Phase 8 Vehicle Detector	I1-8	Preempt 1 In	I15-1
u	Red Rest Mode (Ring 2)	I7-4	Preempt 2 In	I15-2
v	Omit All Red (Ring 2)	I7-7	Preempt 3 In	I15-3
w	Phase 8 Ped Clear	O5-8	Preempt 4 In	I15-4
x	Phase 8 Green	O3-8	Preempt 5 In	I15-5
y	Phase 7 Don't Walk	O4-7	Preempt 6 In	I15-6
z	Phase 6 Don't Walk	O4-6	Alarm 1 Out	O12-7
AA	Phase 6 Ped Clear	O5-6	Alarm 2 Out	O12-8
BB	Phase 6 Check	O7-6	Special Function 1 Out	O13-1
CC	Phase 6 On	O9-6	Special Function 2 Out	O13-2
DD	Phase 6 Next	O8-6	Special Function 3 Out	O13-3
EE	Phase 7 Hold	I3-7	Special Function 4 Out	O13-4
FF	Phase 8 Check	O7-8	Special Function 5 Out	O13-5
GG	Phase 8 On	O9-8	Special Function 6 Out	O13-6
HH	Phase 8 Next	O8-8	Special Function 7 Out	O13-7
JJ	Phase 7 Walk	O6-7	Special Function 8 Out	O13-8
KK	Phase 7 Ped Clear	O5-7	Not Assigned	---
LL	Phase 6 Walk	O6-6	Detector Reset	O11-8
MM	Phase 7 Check	O7-7	Not Assigned	---
NN	Phase 7 On	O9-7	+24 VDC	---
PP	Phase 7 Next	O8-7	2070N DC Gnd	---

TITLE: 2070-8 FILELD I/O MODULE CONECTOR C & D

NO SCALE

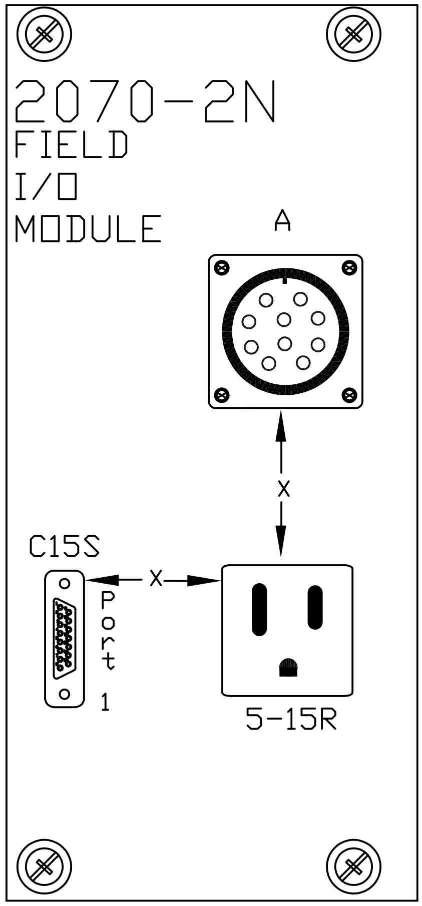
TEES 2008

A11-5

EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD (FCU)
3	RXD (FCU)
4	RTS (FCU)
5	CTS (FCU)
6	NA
7	2070-8 DC GND
8	DCD (FCU)
9	2070-8 DC GND
10	SP3TXD+
11	SP3TXD-
12	SP3TXC+
13	SP3TXC-
14	2070-8 DC GND
15	SP3RXD+
16	SP3RXD-
17	2070-8 DC GND
18	SP3RXC+
19	SP3RXC-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EG (Equipment Ground)
2	TXD (Channel 1)
3	RXD (Channel 1)
4	RTS (Channel 1)
5	CTS (Channel 1)
6	NA
7	IFC GND
8	DCD (Channel 1)
9	AUDIO IN (Channel 1)
10	AUDIO IN (Channel 1)
11	AUDIO OUT (Channel 1)
12	AUDIO OUT (Channel 1)
13	NA
14	EG (Equipment Ground)
15	TXD (Channel 2)
16	RXD (Channel 2)
17	RTS (Channel 2)
18	CTS (Channel 2)
19	NA
20	IFC GND
21	DCD (Channel 2)
22	AUDIO IN (Channel 2)
23	AUDIO IN (Channel 2)
24	AUDIO OUT (Channel 2)
25	AUDIO OUT (Channel 2)

TITLE: 2070-8 FIELD I/O MODULE EX1 & EX2 CONNECTOR	
NO SCALE	A11-6
TEES 2008	



FRONT VIEW

2070-2N FIELD I/O FACE PANEL

A PIN ASSIGNMENT	
PIN	FUNCTION
A	AC Neutral
B	NA
C	AC Line
D	NA
E	NA
F	Fault Monitor
G	DCG #2
H	EG
I	NA
J	NA

C15S PIN ASSIGNMENT	
PIN	FUNCTION
1	SP3TXD+
2	DCG #2
3	SP3TXC+
4	DCG #2
5	SP3RXD+
6	DCG #2
7	SP3RXC+
8	DCG #2
9	SP3TXD-
10	Port 1 Disable
11	SP3TXC-
12	EG
13	SP3RXD-
14	Reserved
15	SP3RXC-

Notes (This detail)

1. 2070N Faceplate shall be 4X wide.
2. RS-485 Termination Resistors (120 Ohms) provided external to module.
3. Dimension "X" shall be minimum of 1.00 in.
4. A - Intermate with MS3106()-18-1S.
   C15S - 15-Pin DB Socket Type.
5. EG (Equipment Ground) pin is electrically connected to the faceplate.
6. Port 1 Disable: 0VDC = Disable.

TITLE: MODEL 2070-2N FILELD I/O MODULE	
NO SCALE	A11-7
TEES 2008	